

Compal Confidential

Intel M/B Schematics Document

Kabylake-U(2+2)-DDR4 SODIMMx2

nVidia N16 gDDR5-2GB

(N16S-GTR : GM108-670/770: GeForce MX130)

(N16V-GMR1 : GM108-626/726: GeForce MX110)

Project :2018OPP_Harry Potter(15.6")

EPW50 :LA-G07FP

Date : 2018-01-08

Version : 1.0

(Modified&Ref from:
01."NFLC_KBLR_LAE802PR10_MV_FINAL")

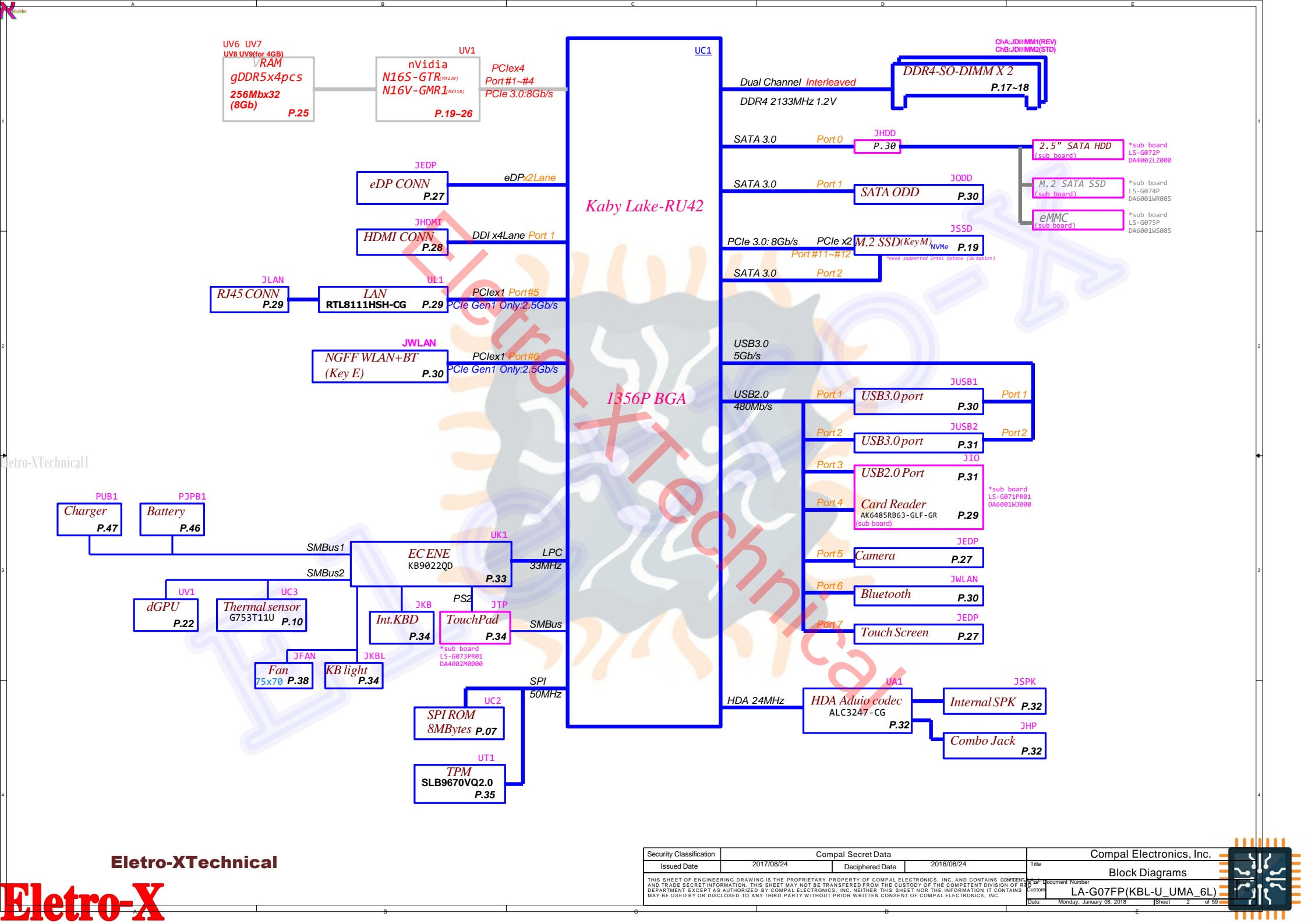
(02."Canadiens_LA-F055P-R10-KBL-ON-2017-06-23_CPU")
(02."CNL-U ORB_DDX02_LA-F152PR01_0822B")

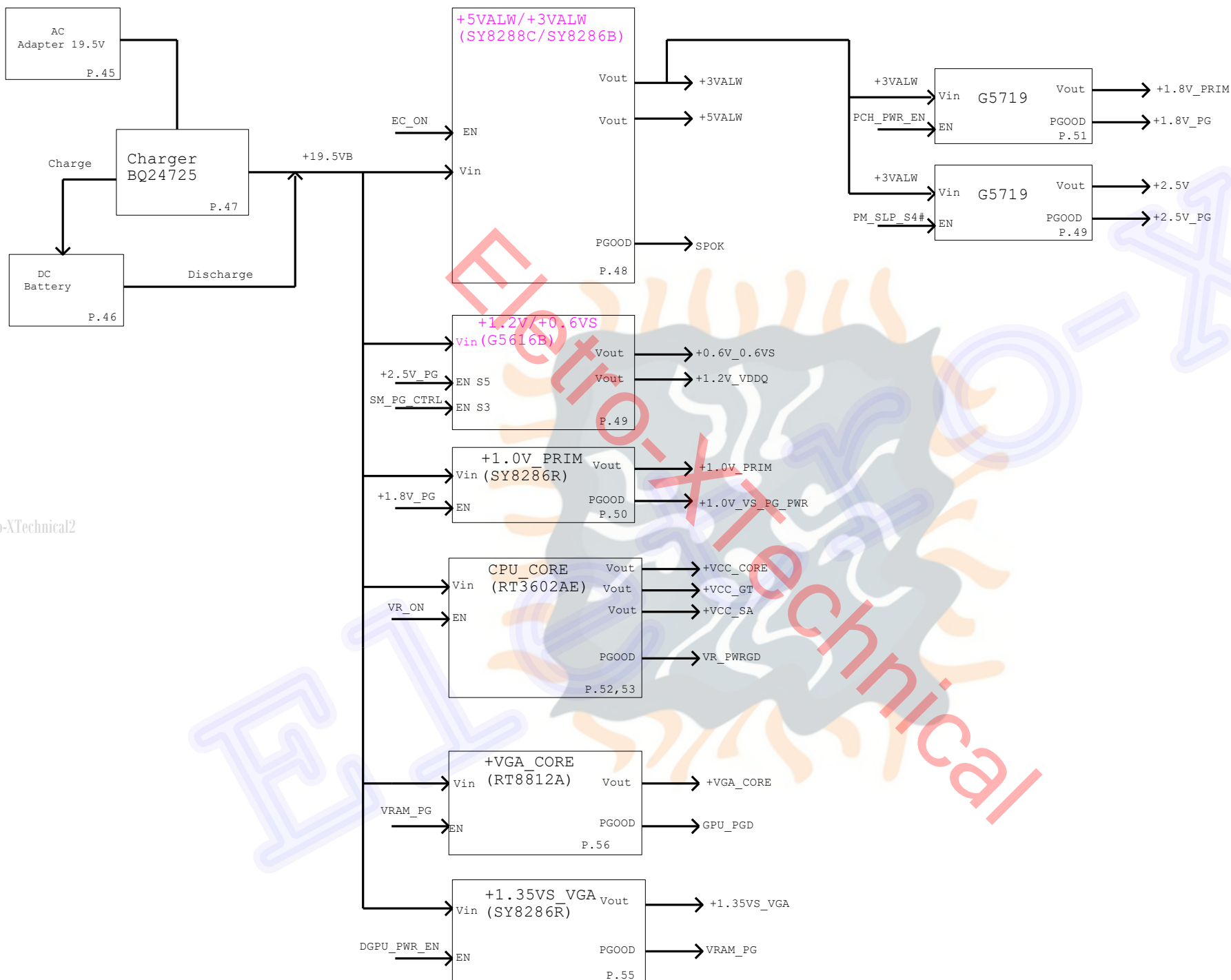
Eletro-XTechnical

Eletro-X

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| | | | | Date: | Monday, January 08, 2018 |
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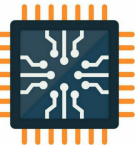
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| | | | | Rev 0.3 |
| | | | | LA-G07FP(KBL-U_UMA_6L) |
| | | | | Friday, January 05, 2018 |
| | | | | Sheet 58 of 58 |

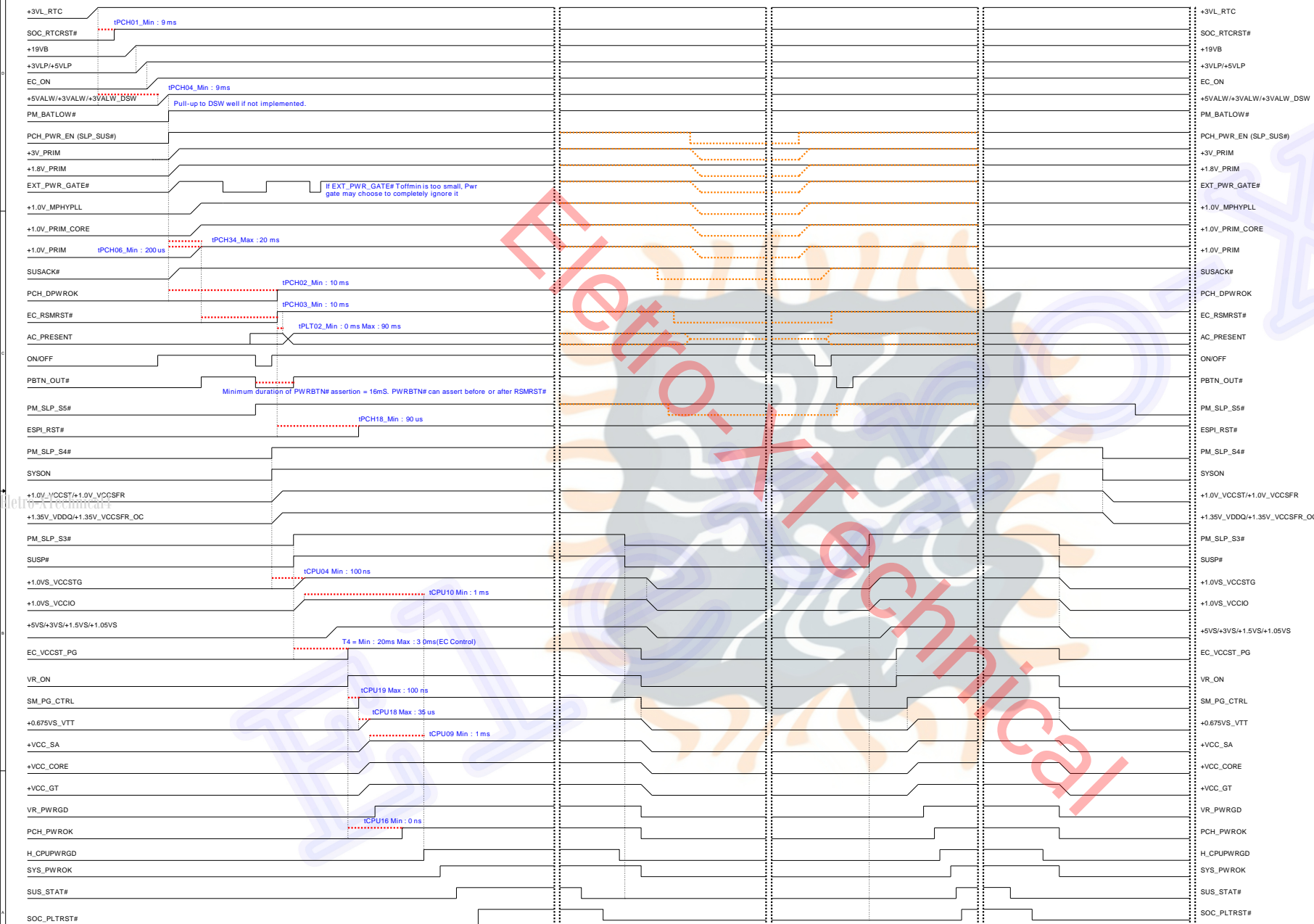


G3->S0

S0->S3/DS3

S0/DS3->S0

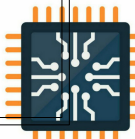
S0->S5



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Eletro-X

| | | | | | |
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| Issued Date | Design Date | Title | | HW Reserve | |
| Customer | Document Number | LA-G07/FP(KBL-U_UMA_6L) | Rev | V0.3 | |
| Model | Family | 2200G/10/10/10/10 | Device | Eletro-X | |



SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

1 = Port Bis detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.

HDMI DDC (Port B)

<28> HOST_DP1_CTRL_CLK
<28> HOST_DP1_CTRL_DATA

HOST_DP1_CTRL_CLK L13
HOST_DP1_CTRL_DATA L12

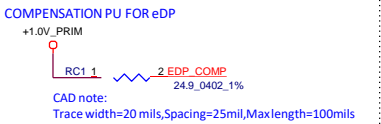
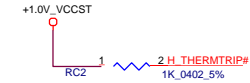
SKL-U_BGA1356

1 OF 20

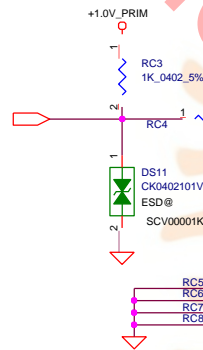
HOST_DP1_HPD <28> From HDMI
TP@ T408
NMI_DBG#_CPU <10,33>
EC_SC# <33>
EDP_HPD <27> From eDP

EDP_BKLTEN
EDP_BKLTCTL
EDP_VDDEN

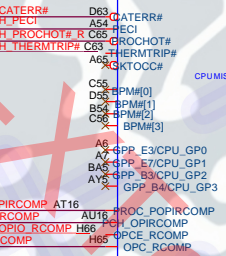
ENBKIL <33>
BKL_PWM_CPU <27>
ENVDD_CPU <27>



<33> PROCHOT#



T248 TP@ CATERR#
H_PECI
H_PROCHOT# R C65
H_THERMTRIP# C63

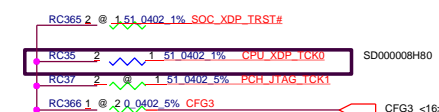
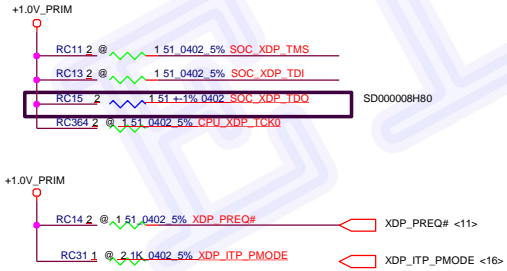


SKL-U_BGA1356

PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX

RC123 1 @ 2 100K 0.402 5% ENVDD_CPU
RC124 1 @ 2 100K 0.402 5% ENBKIL

XDP CONN



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| Date: | Friday, January 05, 2018 | Sheet | 5 of 5 |

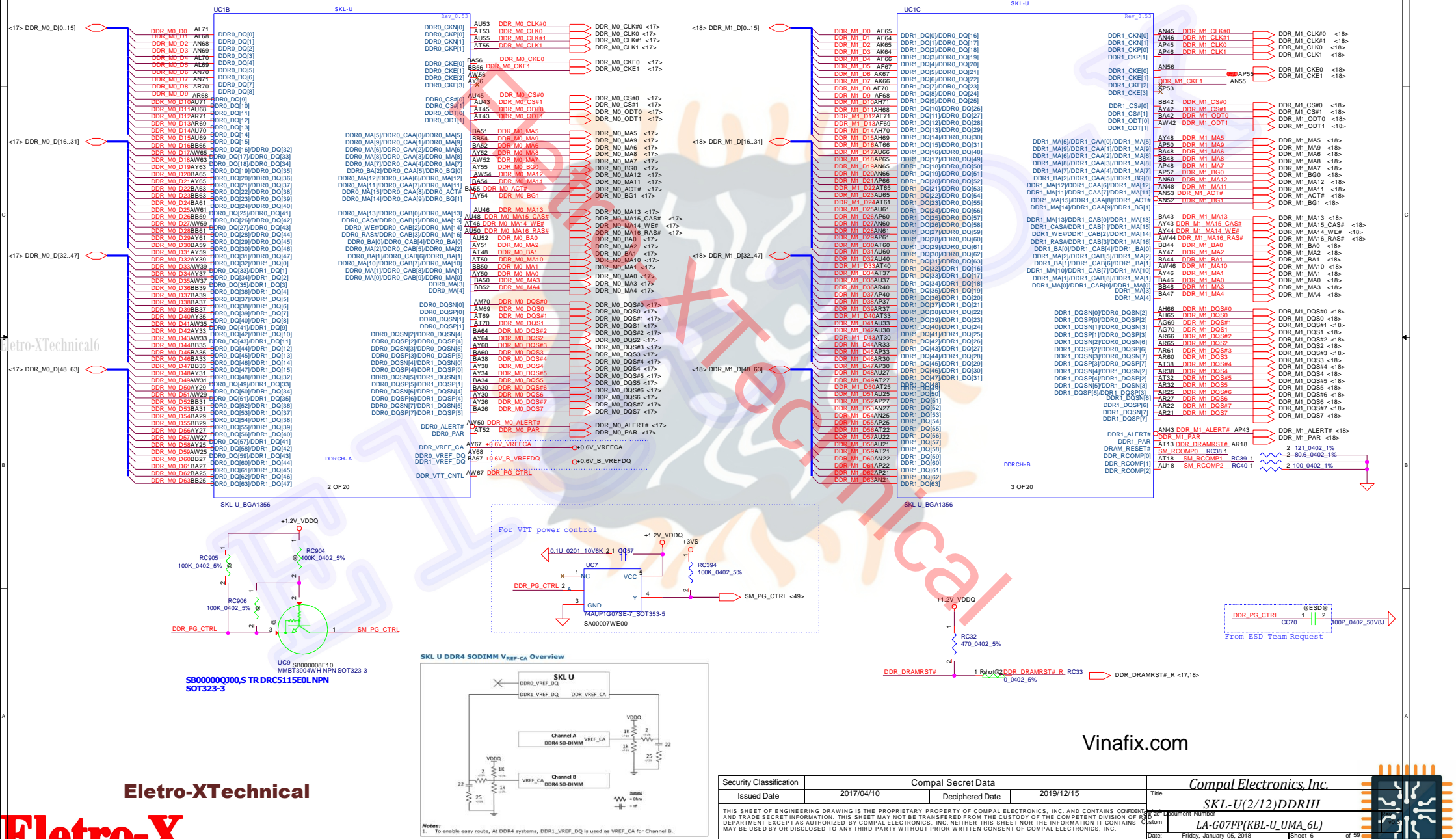


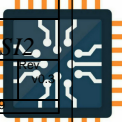
Interleaved Memory

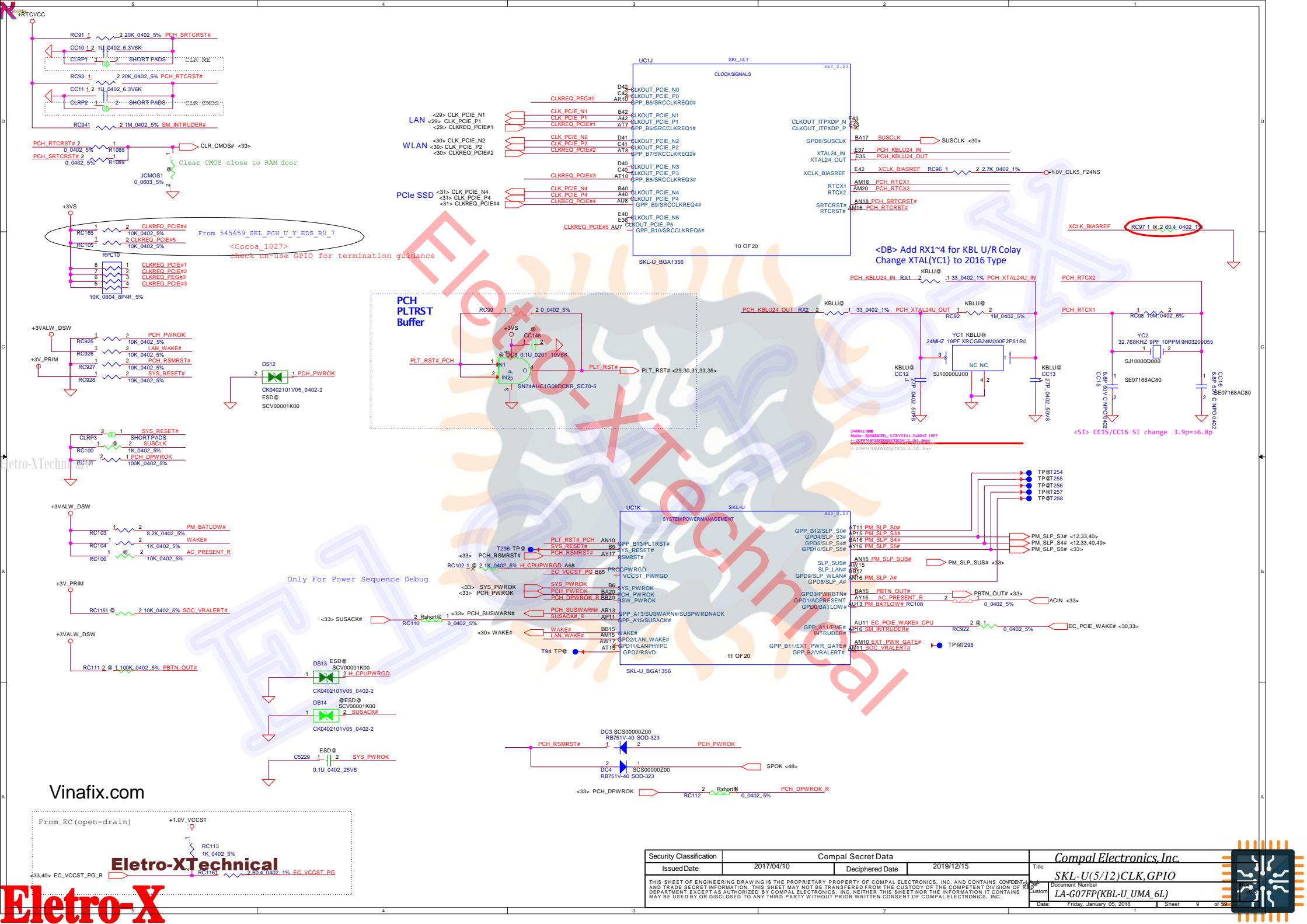
Interleaved Memory

<Cocoa_1020>

PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)







Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.----> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

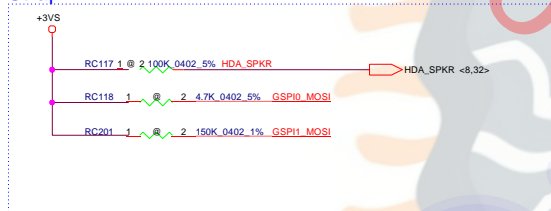
GSPI1_MOSI (Internal Pull Down):

Boot BIOS StrapBit

0 = SPI Mode --> AAX05 Use

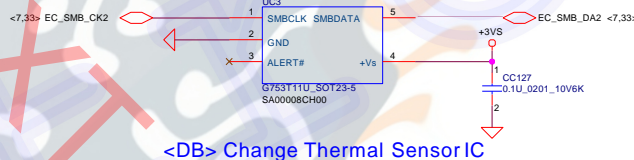
1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR

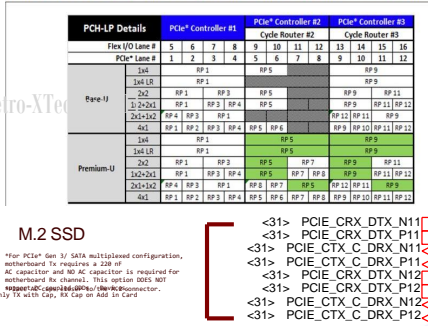
Address : 0x48



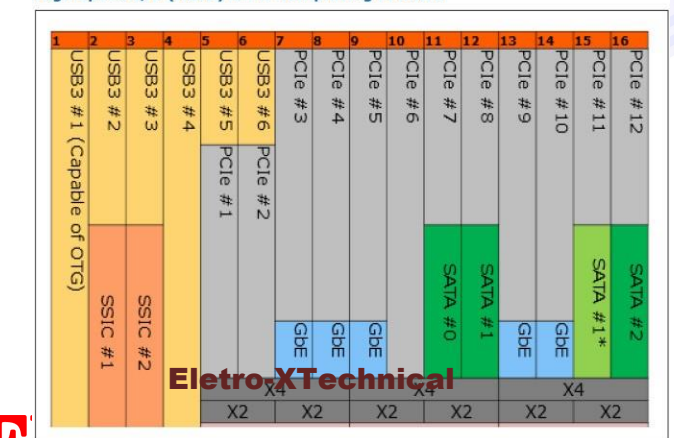
<DB> Change Thermal Sensor IC

LAN
WLAN
HDD
ODD

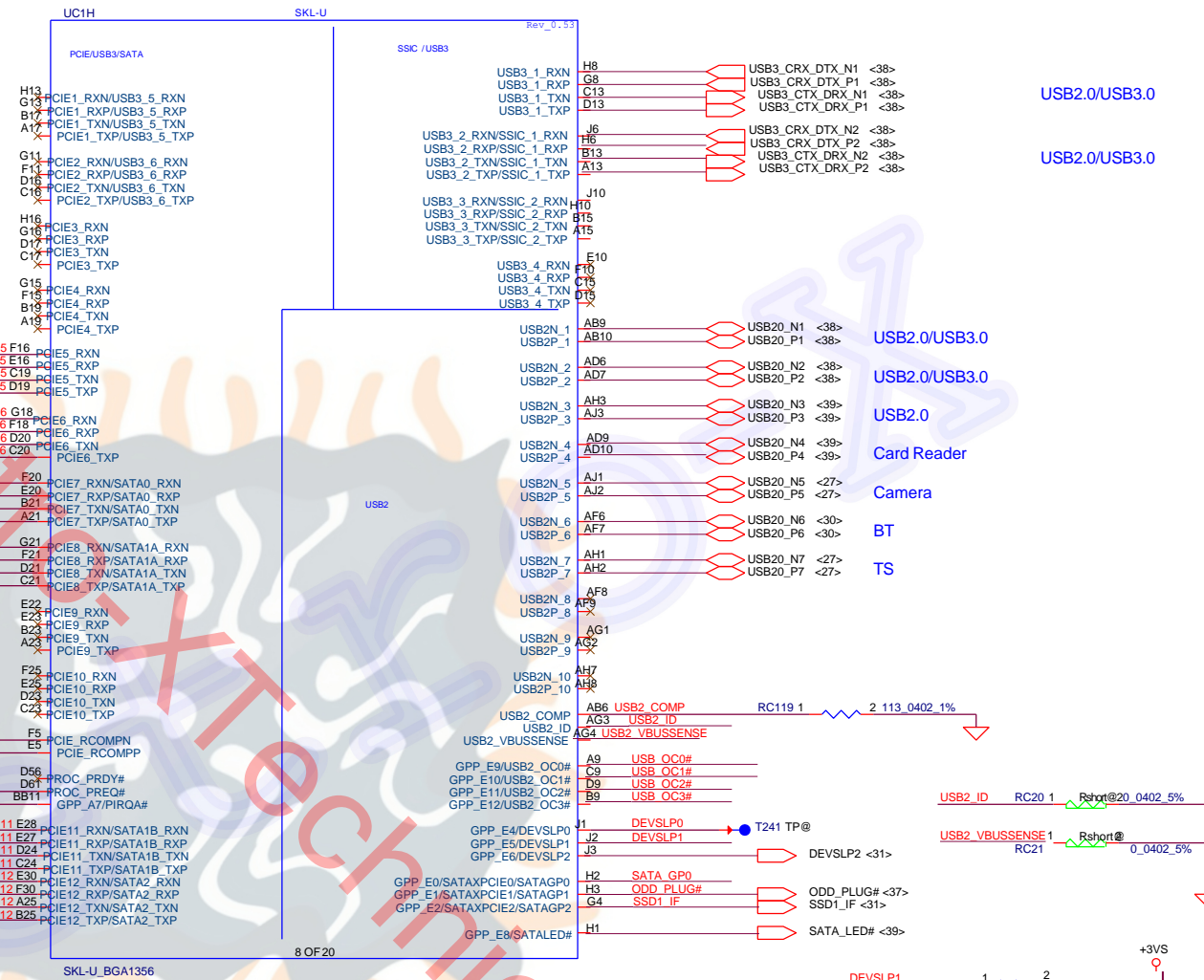
Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter



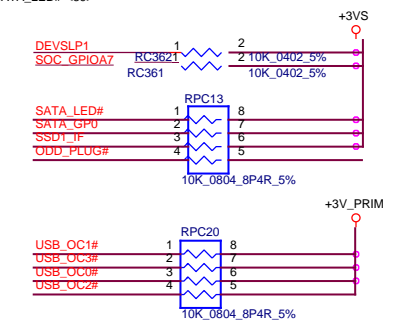
High Speed I/O (HSIO) Lane Multiplexing in SKL-U



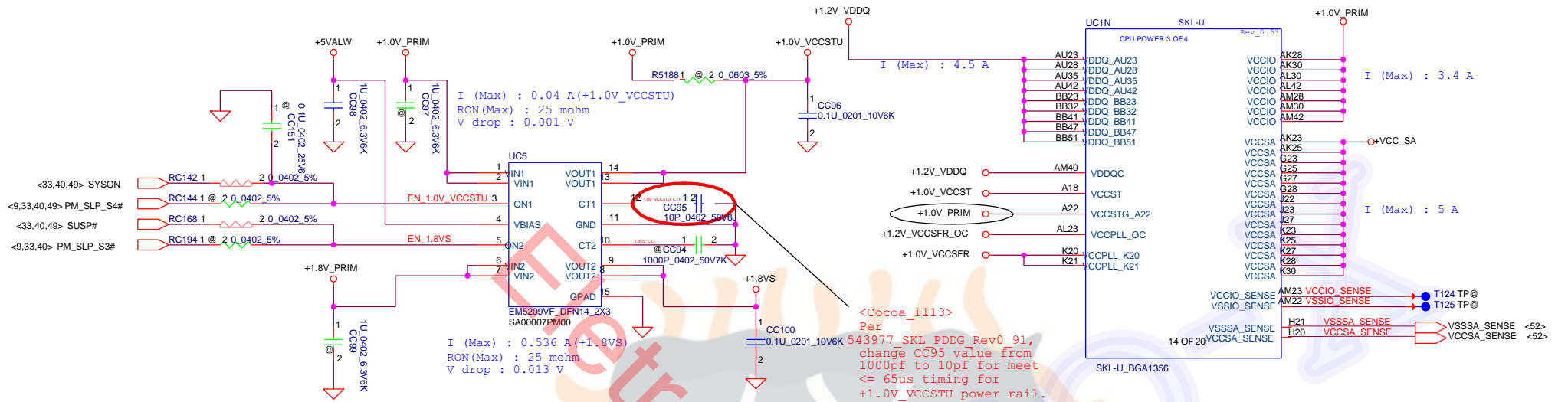
When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.



| GPIO | DEVICE CONTROL |
|----------|------------------------|
| USB_OC0# | USB2 Port 1 and Port 2 |
| USB_OC1# | USB2 Port 3 |
| USB_OC2# | N/A |
| USB_OC3# | N/A |
| DEVSLP0 | N/A |
| DEVSLP1 | N/A |
| DEVSLP2 | NGFF SSD KEY- M |
| SATA_GP0 | N/A |
| SATA_GP1 | ODD_PLUG# |
| SATA_GP2 | PCIE/SATA |

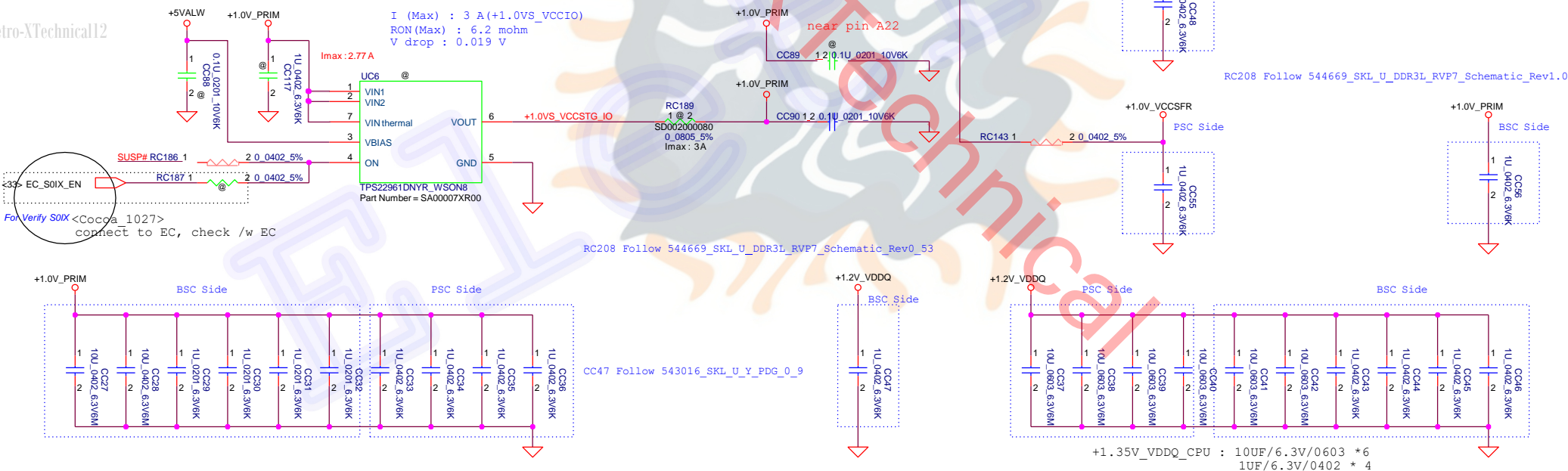


+1.0V_PRIM TO +1.0V_VCCSTU



Vinafix.com

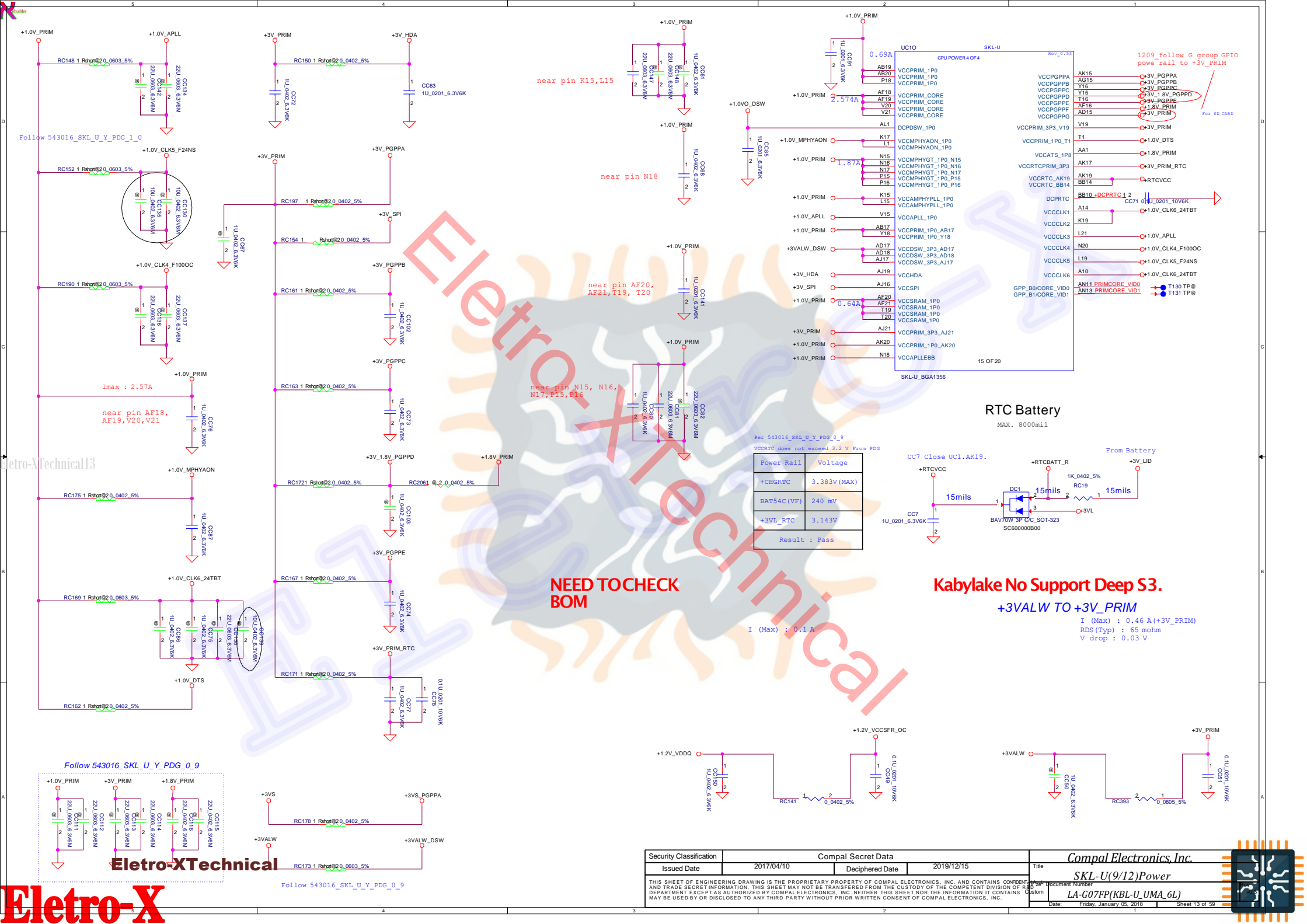
+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

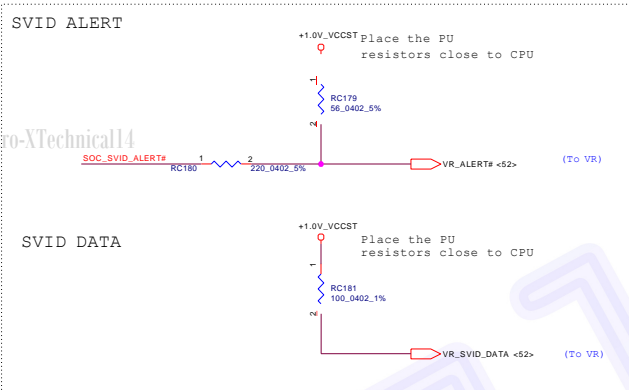


Eleto-XTechnical

Eletro-X

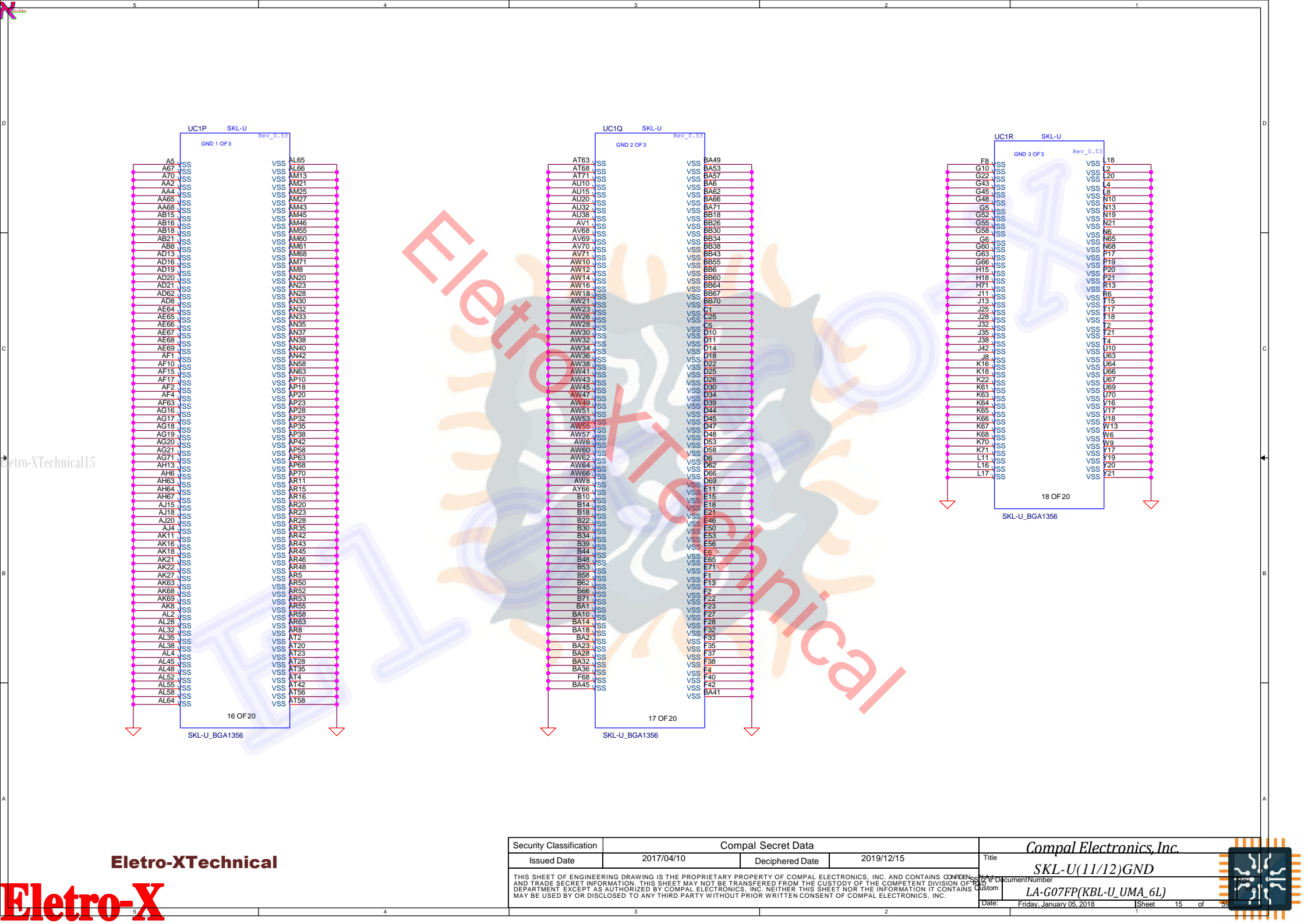
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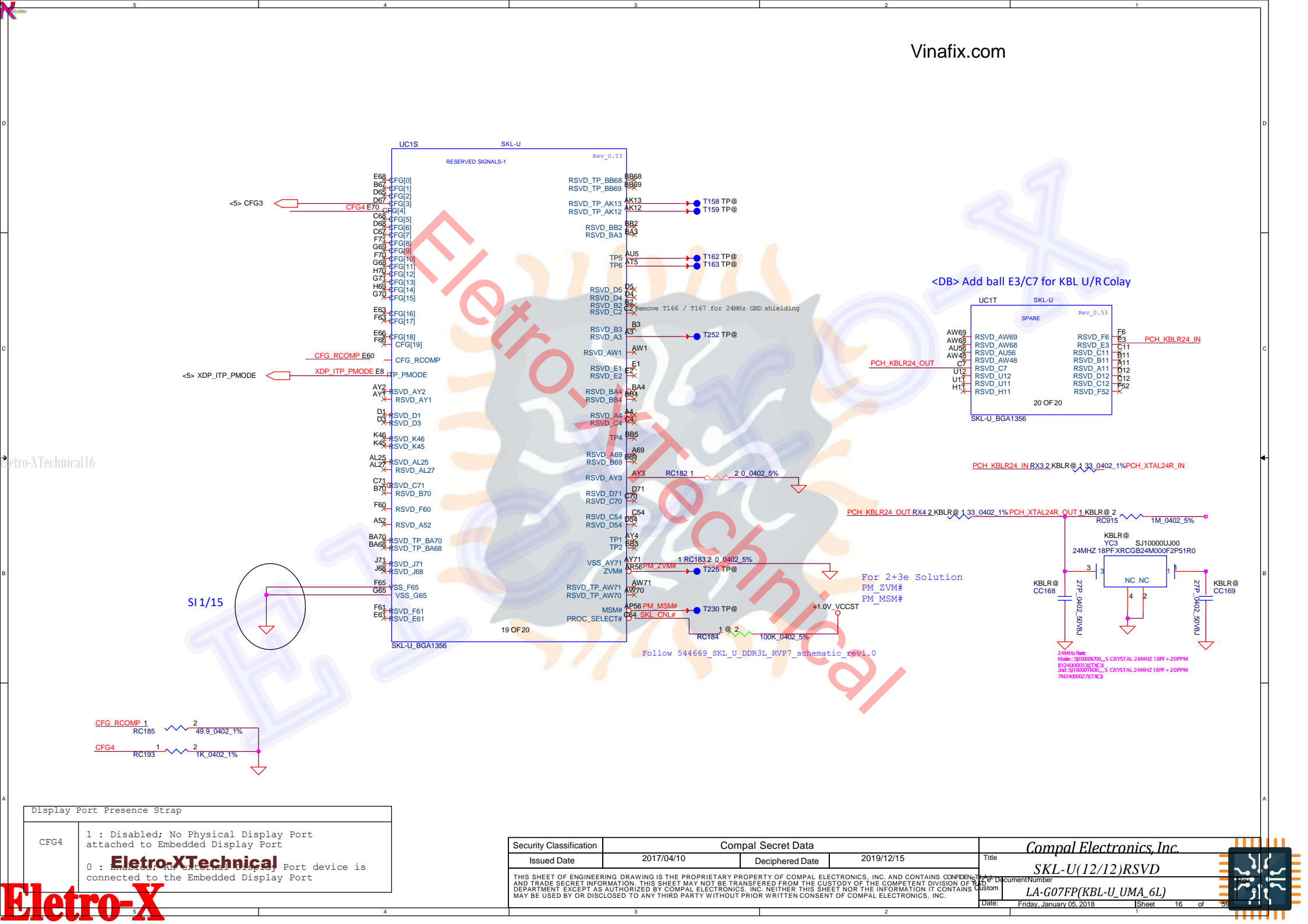




Eletr-X Technical

Eletr-X

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| | | | | Date: | Friday, January 05, 2018 |
| | | | | Sheet | 15 of 15 |

[illegible][illegible]

REVERSE TYPE

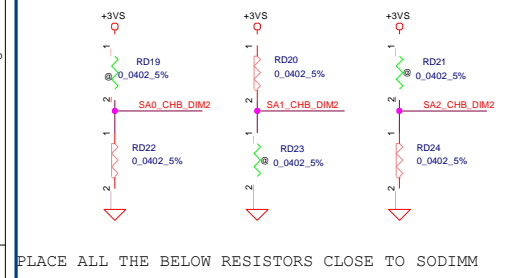
Interleaved Memory

CHANNEL-B

STD (5.2 mm)

Interleaved Memory

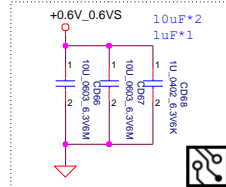
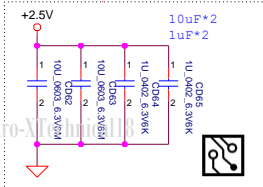
TOP: JDIMM2 CONN Non-ECC DIMM



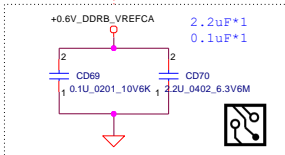
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.258

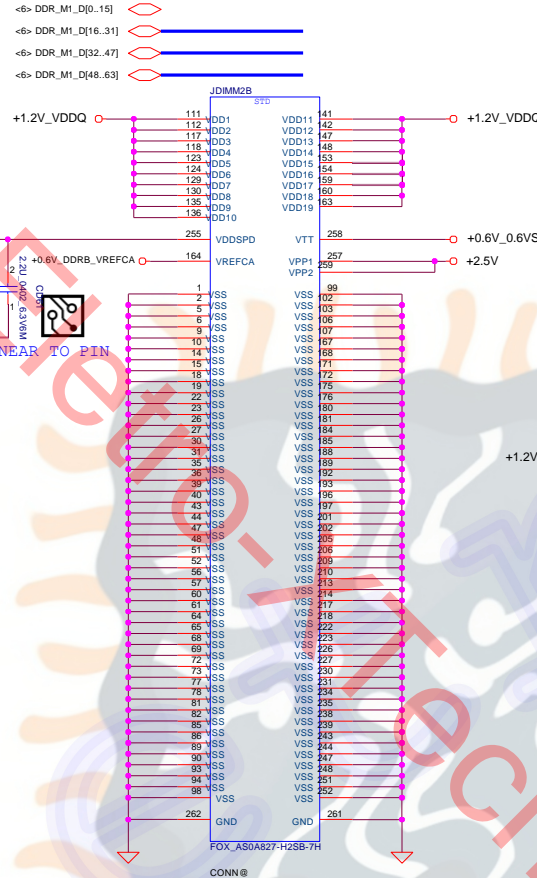
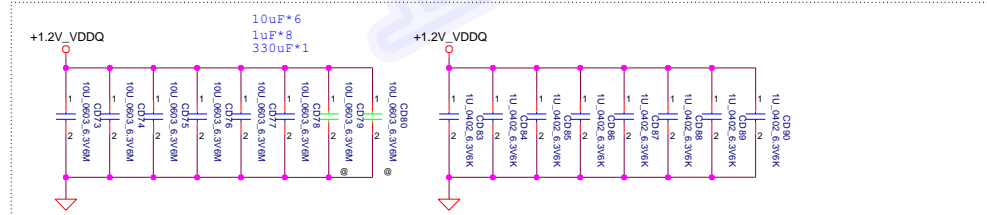


Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

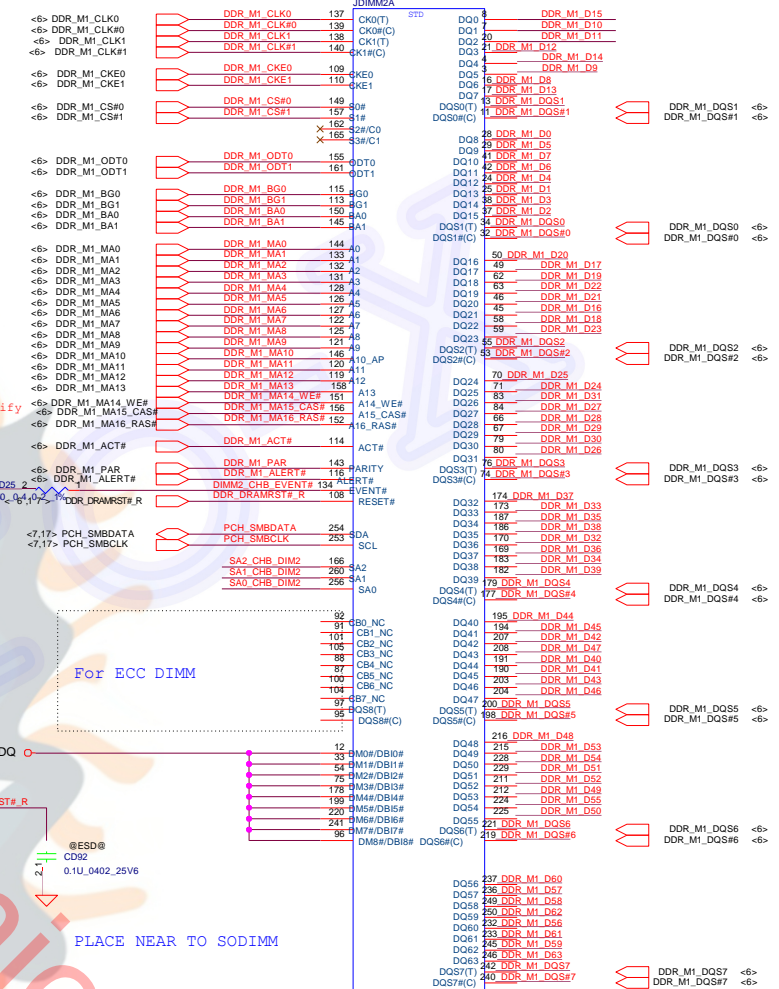
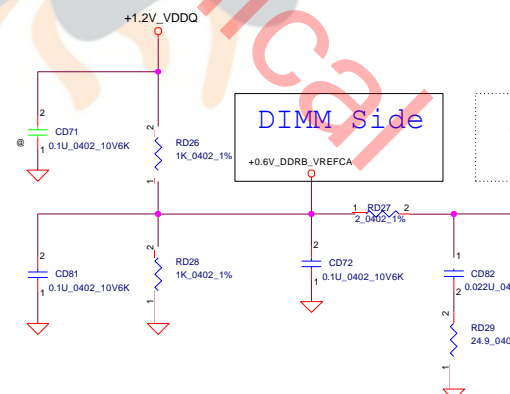


Layout Note:
Place near JDIMM2

Vinafix.com



Part Number: LTCX0069FA0
Part Value: S SOCKET FOX AS0A827-H2SB-7H 260P DDR4



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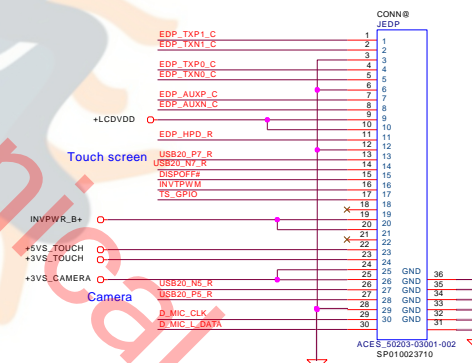
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| Date | | Friday, January 05, 2018 | |
| Sheet | | 18 of | |

Camera



Eletro-X



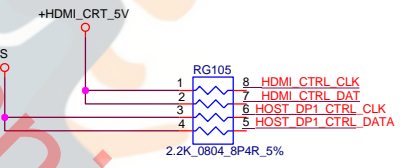
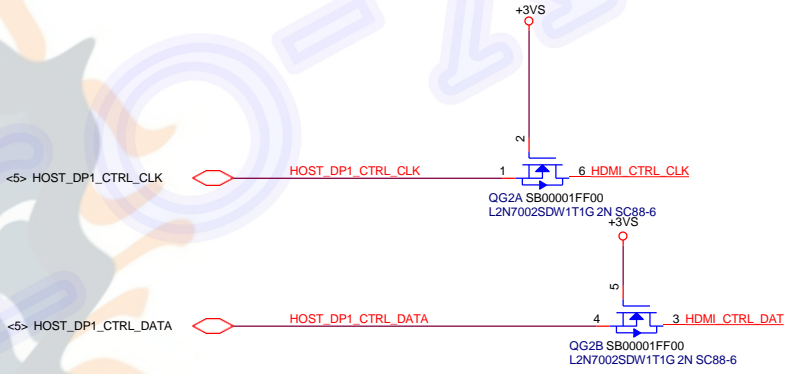
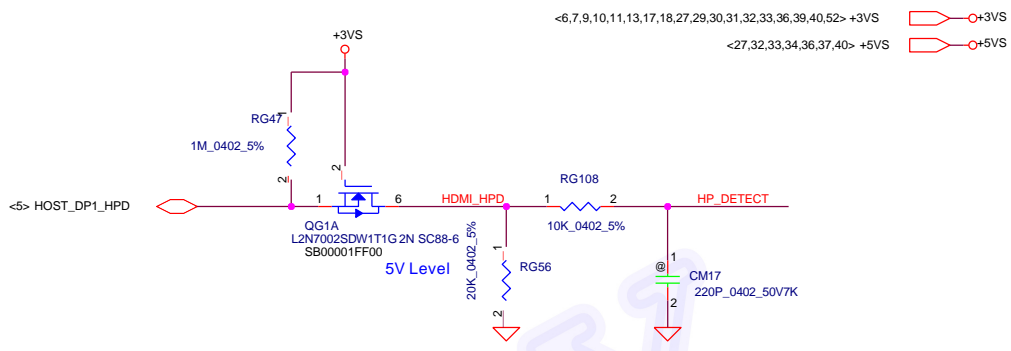
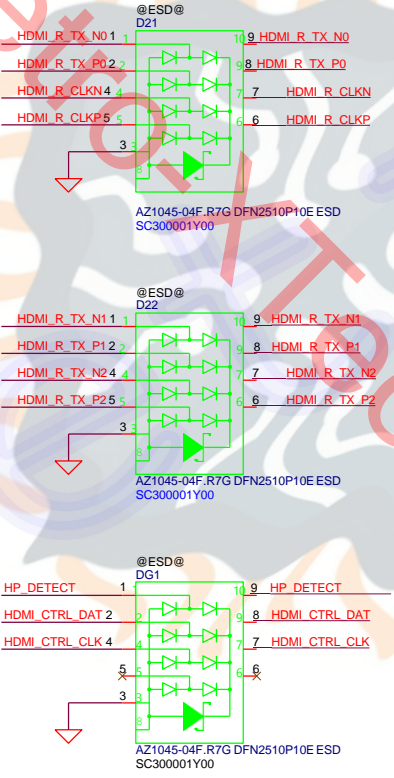
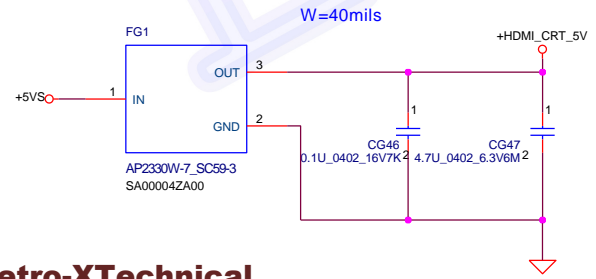
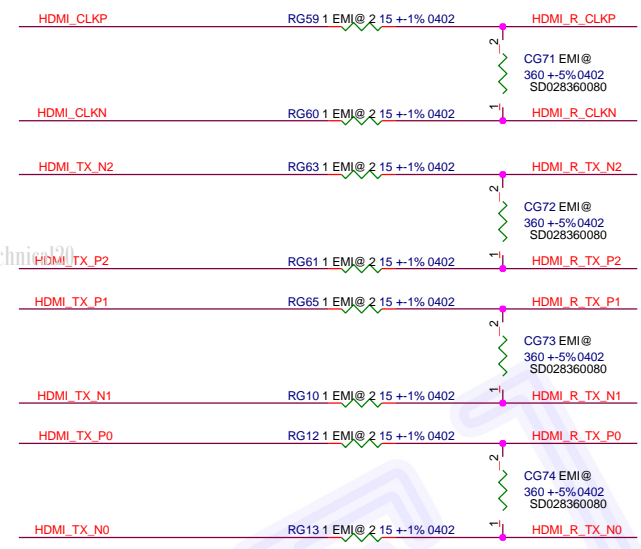
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| | | | | Date | Friday, January 05, 2018 |
| | | | | Sheet | 27 of 50 |

1.3.2 Digital Display Interface Signal Mapping

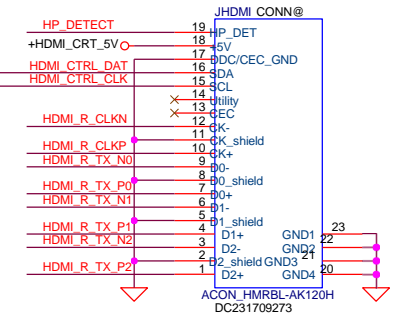
Table 1-4. Digital Display Interface Signal Mapping

| Port | DDI PROCESSOR Pin Names | Display Port Mapping | HDMI* Mapping |
|--------|-------------------------|----------------------|----------------|
| Port 1 | DDI1_TXN[0] | DDI1_LANE0_DN | HDMI0C_TX2_DN |
| | DDI1_TXP[0] | DDI1_LANE0_DP | HDMI0C_TX2_DP |
| | DDI1_TXN[1] | DDI1_LANE1_DN | HDMI0C_TX1_DN |
| | DDI1_TXP[1] | DDI1_LANE1_DP | HDMI0C_TX1_DP |
| | DDI1_TXN[2] | DDI1_LANE2_DN | HDMI0C_TX0_DN |
| | DDI1_TXP[2] | DDI1_LANE2_DP | HDMI0C_TX0_DP |
| | DDI1_TXN[3] | DDI1_LANE3_DN | HDMI0C_CLK_DN |
| | DDI1_TXP[3] | DDI1_LANE3_DP | HDMI0C_CLK_DP |
| | DDPB_HPD | DDI1_HPD_Q | DDI1_HPD_Q |
| | DDPB_CTRLCLK | NA | DDI1_CTRL_CLK |
| | DDPB_CTRLDATA | NA | DDI1_CTRL_DATA |
| | DDPB_CTRLDATA | NA | DDI1_CTRL_DATA |

*DDA30_LA-F292PR02: RS_8.2ohm_RP_360ohm

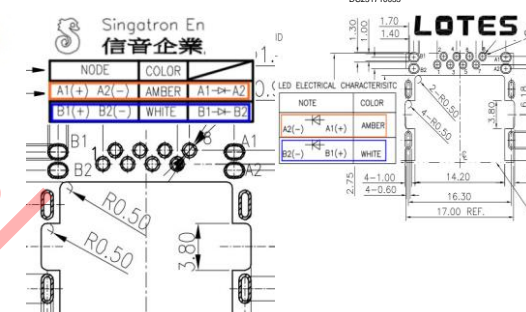
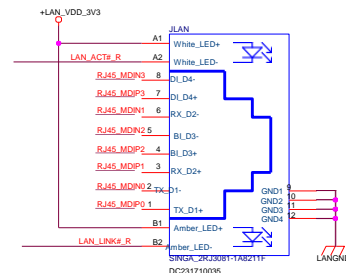
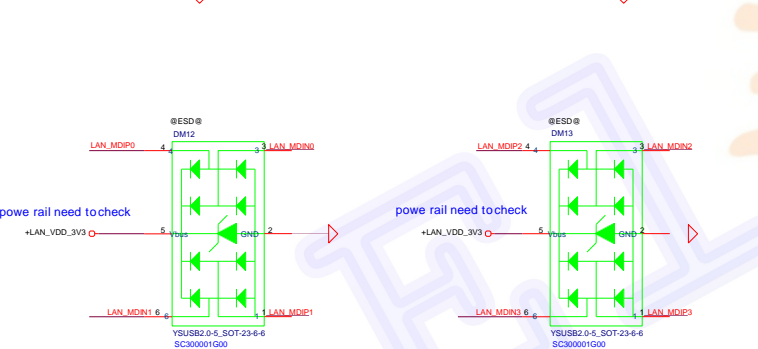
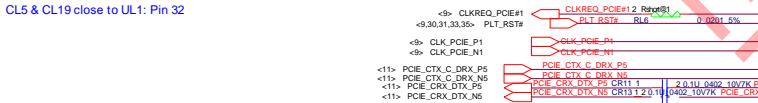
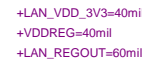
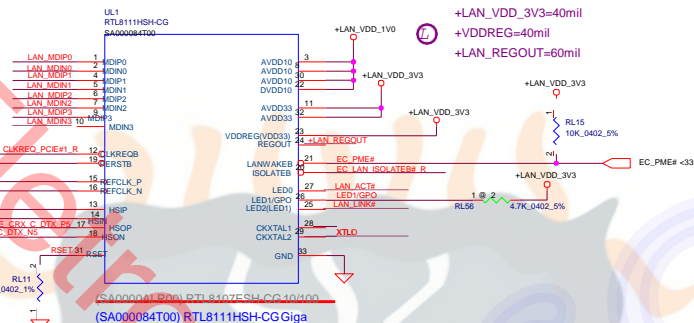
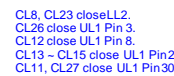


HDMI Conn.



Eletro-XTechnical

Eletro-X



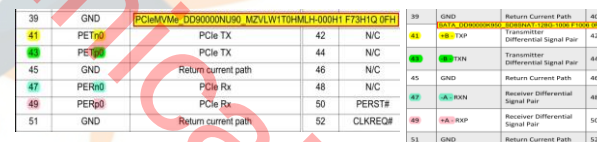


Unpop QB8 and RL25 for not support OBFF



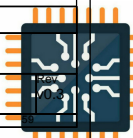


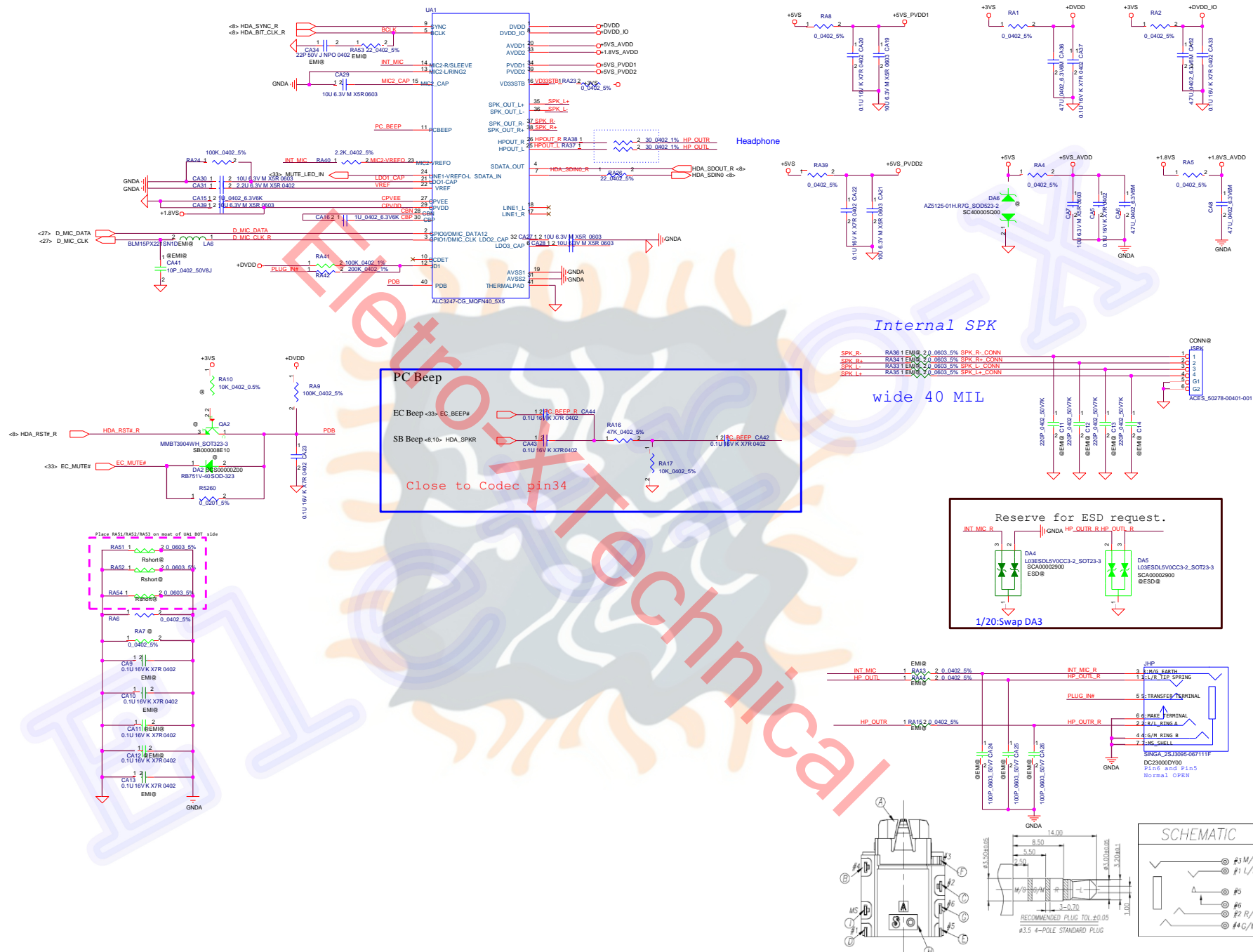
| PCH-LR Details | | | | PCIe* Controller #1 | | | | PCIe* Controller #2 | | | | PCIe* Controller #3 | | | |
|-----------------|---------|------|------|---------------------|-----------|------|------|---------------------|------------------|------|-------|---------------------|-------|----|----|
| Flex I/O Lane # | | | | 5 | 6 | 7 | 8 | Cycle Router #2 | | | | Cycle Router #3 | | | |
| PCIe* Lane # | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| Base-U | 1x4 | RP 1 | | | RP 5 | | | | RP 9 | | | | | | |
| | 1x4 LR | RP 1 | | | | | | | RP 9 | | | | | | |
| | 2x2 | RP 1 | RP 3 | | RP 5 | | | | RP 9 RP 11 | | | | | | |
| | 1x2+2x1 | RP 1 | RP 3 | RP 4 | RP 5 | | | | RP 9 RP 11 RP 12 | | | | | | |
| | 2x1+1x2 | RP 4 | RP 3 | RP 1 | | | | | RP 12 RP 11 RP 9 | | | | | | |
| | 4x1 | RP 1 | RP 2 | RP 3 | RP 4 | RP 5 | RP 6 | | | RP 9 | RP 10 | RP 11 | RP 12 | | |
| Premium-U | 1x4 | RP 1 | | | RP 5 | | | | RP 9 | | | | | | |
| | 1x4 LR | RP 1 | | | RP 5 | | | | RP 9 | | | | | | |
| | 2x2 | RP 1 | RP 3 | | RP 5 RP 7 | | | | RP 9 RP 11 | | | | | | |
| | 1x2+2x1 | RP 1 | RP 3 | RP 4 | RP 5 RP 7 | | | | RP 9 RP 11 RP 12 | | | | | | |
| | 2x1+1x2 | RP 4 | RP 3 | RP 1 | RP 8 | RP 7 | RP 5 | RP 12 RP 11 RP 9 | | | | | | | |
| | 4x1 | RP 1 | RP 2 | RP 3 | RP 4 | RP 5 | RP 6 | RP 7 | RP 8 | RP 9 | RP 10 | RP 11 | RP 12 | | |

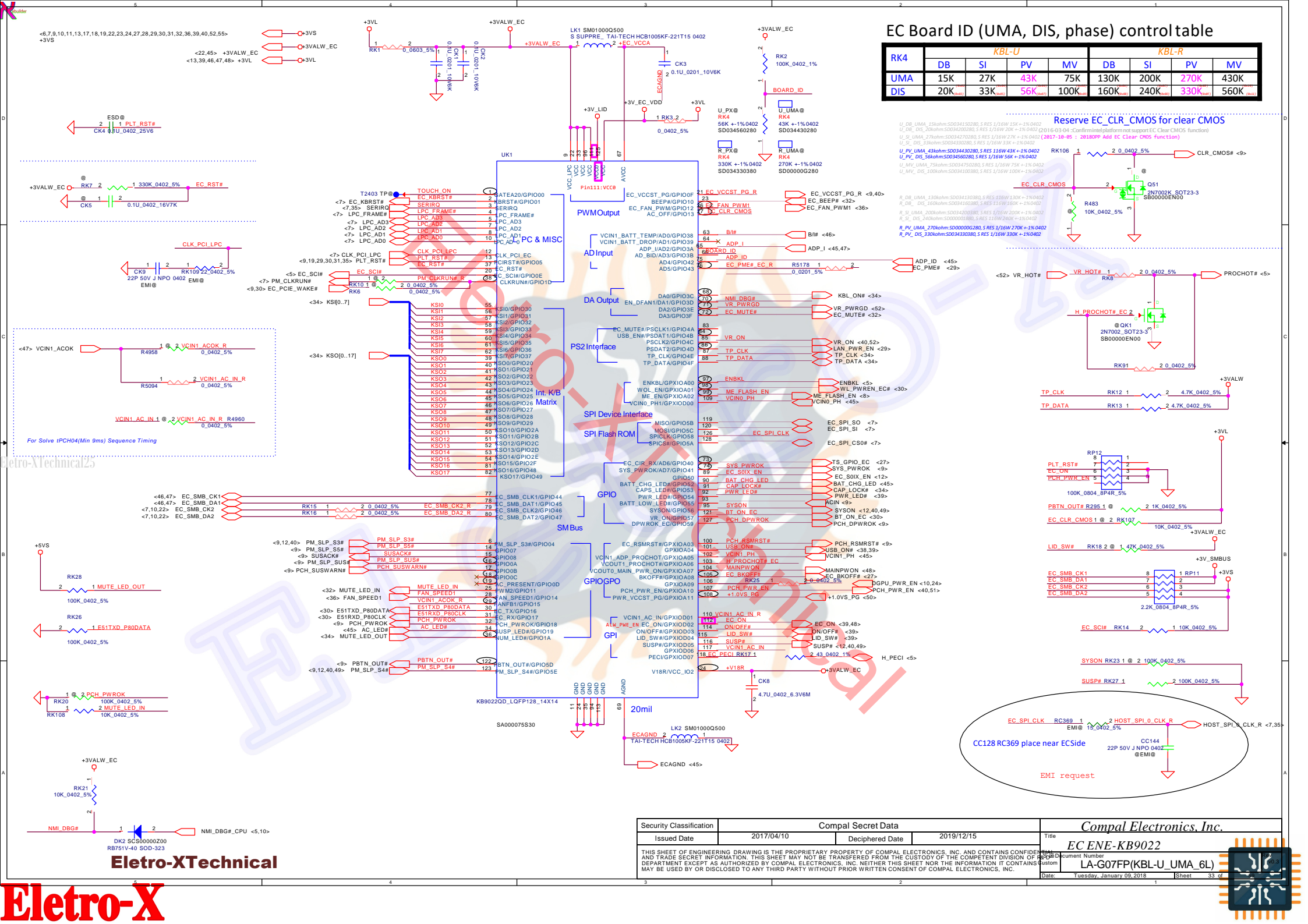


The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.







EC Board ID (UMA, DIS, phase) control table

| RK4 | KBL-U | | | | KBL-R | | | |
|-----|-------|-----|-----|------|-------|------|------|------|
| | DB | SI | PV | MV | DB | SI | PV | MV |
| UMA | 15K | 27K | 43K | 75K | 130K | 200K | 270K | 430K |
| DIS | 20K | 33K | 56K | 100K | 160K | 240K | 330K | 560K |

Reserve EC_CLR_CMOS for clear CMOS

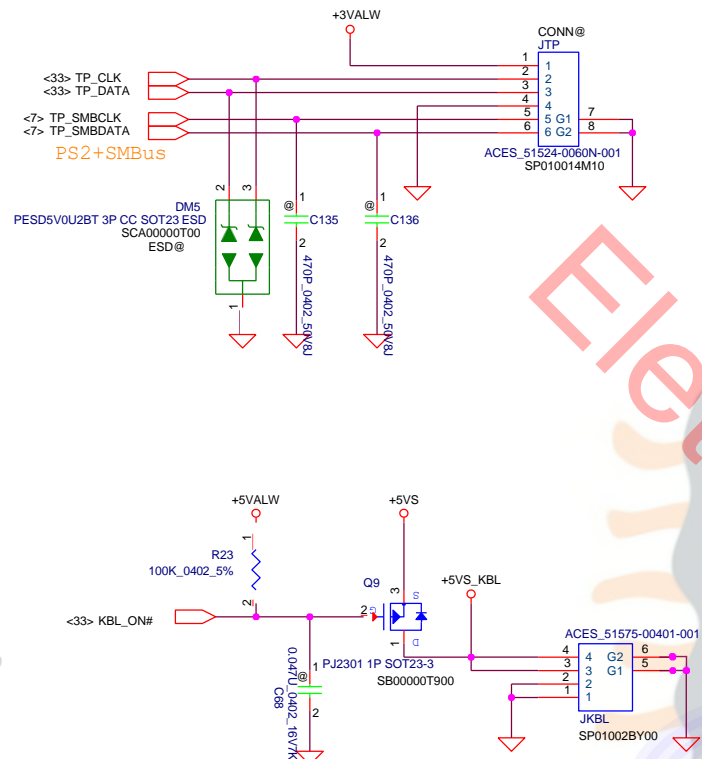
U_DB_UMA_150kOhm:SD034130280,5 RES 1/16W 15K +/-1% 0402
U_DB_DIS_200kOhm:SD034130280,5 RES 1/16W 20K +/-1% 0402
U_SI_UMA_270kOhm:SD034130280,5 RES 1/16W 27K +/-1% 0402
U_SI_DIS_330kOhm:SD034130280,5 RES 1/16W 33K +/-1% 0402
U_PV_UMA_430kOhm:SD034130280,5 RES 1/16W 43K +/-1% 0402
U_PV_DIS_560kOhm:SD034130280,5 RES 1/16W 56K +/-1% 0402
U_MV_UMA_750kOhm:SD034130280,5 RES 1/16W 75K +/-1% 0402
U_MV_DIS_100kOhm:SD034130280,5 RES 1/16W 100K +/-1% 0402
R_DB_UMA_130kOhm:SD034130280,5 RES 1/16W 130K +/-1% 0402
R_DB_DIS_160kOhm:SD034130280,5 RES 1/16W 160K +/-1% 0402
R_SI_UMA_200kOhm:SD034130280,5 RES 1/16W 200K +/-1% 0402
R_SI_DIS_240kOhm:SD034130280,5 RES 1/16W 240K +/-1% 0402
R_PV_UMA_270kOhm:SD034130280,5 RES 1/16W 270K +/-1% 0402
R_PV_DIS_330kOhm:SD034130280,5 RES 1/16W 330K +/-1% 0402

Eleto-X Technical

Eleto-X

| | | | | |
|--|---------------------------|-----------------|------------|---|
| Security Classification | Compal Secret Data | | Title | |
| Issued Date | 2017/04/10 | Deciphered Date | 2019/12/15 | EC ENE-KB9022 |
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| Date | Tuesday, January 09, 2018 | Sheet | 33 of 33 | |

TP Button BD Connector



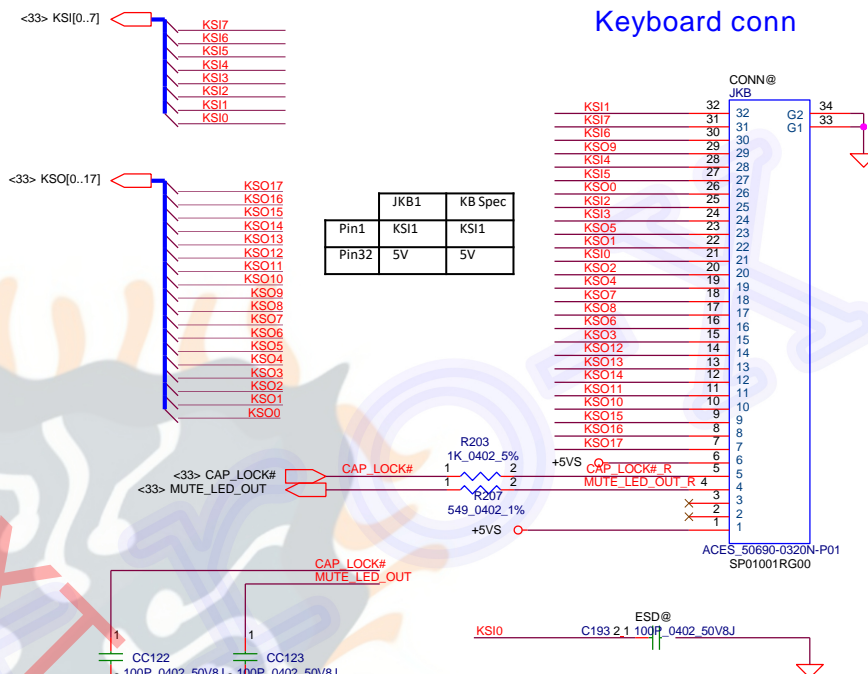
<7,13,29,30,33,35,40,48,49,50,51> +3VALW

<12,37,38,39,40,48,49,52,53> +5VALW

<33> KSI[0..7]

<33> KSO[0..17]

Keyboard conn



| Pin1 | Pin32 | KB1 | KB Spec |
|------|-------|------|---------|
| | | KSI1 | KSI1 |
| | | 5V | 5V |

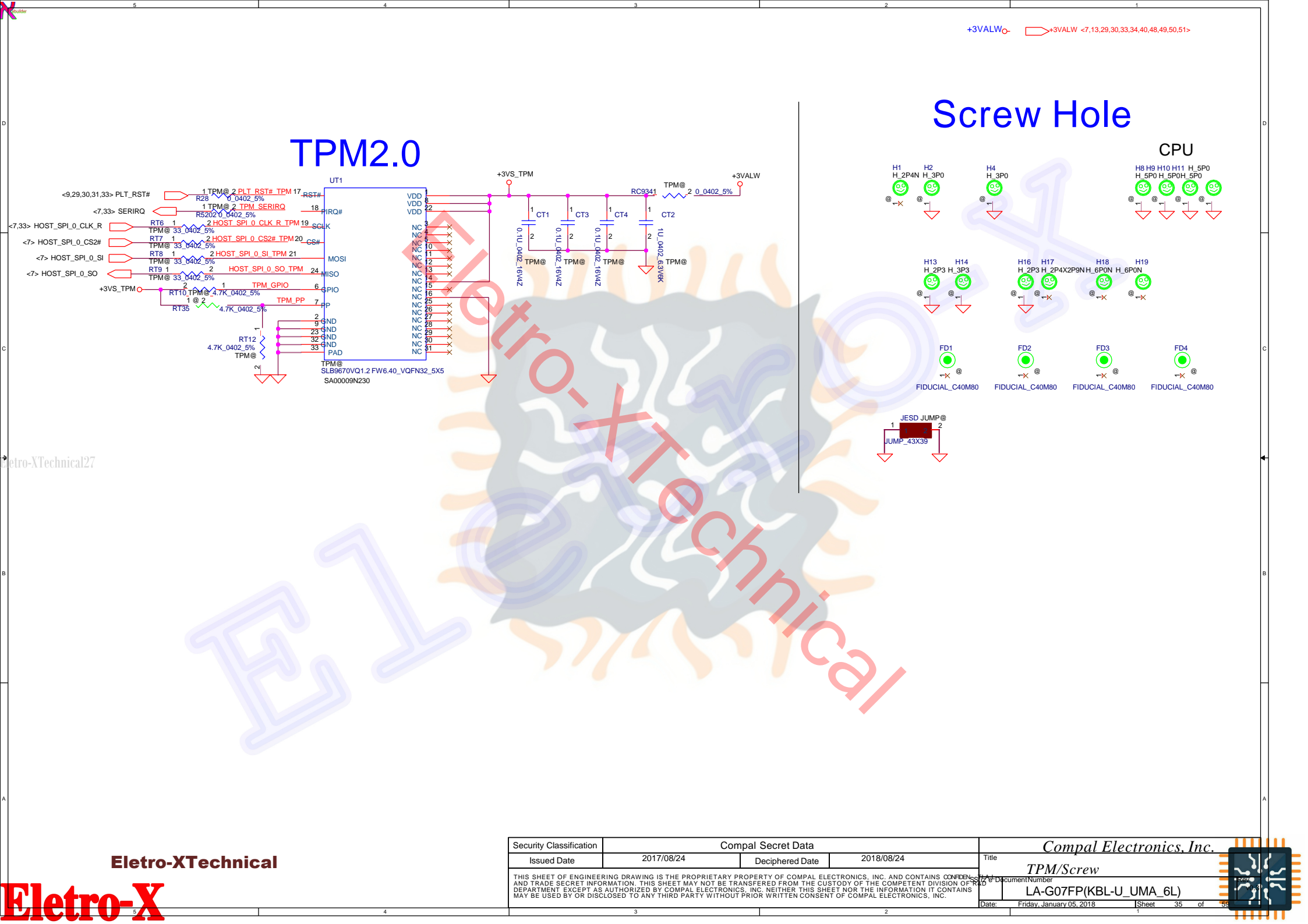
Eleto-XTechnical26

Eleto-XTechnical

Eleto-X

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| | | | | LA-G07FP(KBL-U_UMA_6L) |
| | | | | Date: Friday, January 05, 2018 |
| | | | | Sheet 34 of 59 |



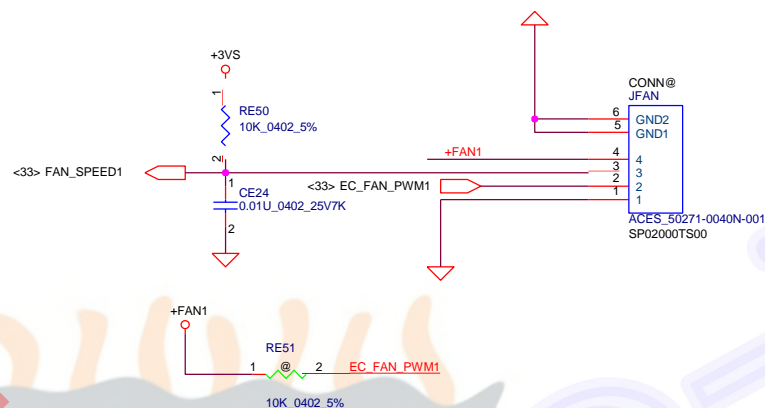
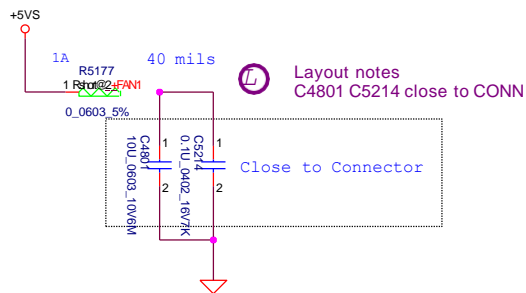


TPM2.0

Screw Hole

CPU

| | | | | | |
|---|------------|--------------------|------------|--------------------------|--------------------------|
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| | | | | Date | Friday, January 05, 2018 |
| | | | | Sheet | 35 of 35 |



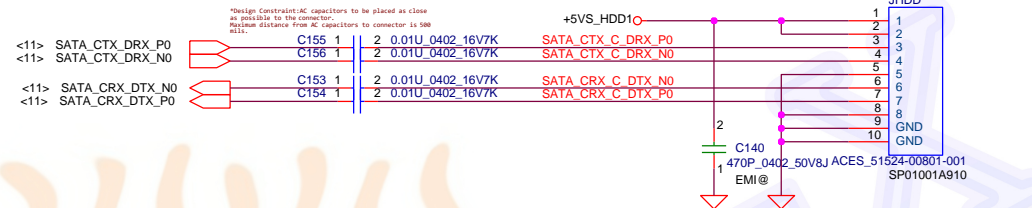
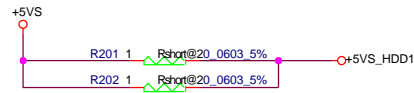
Eletro-XTechnical

Eletro-X

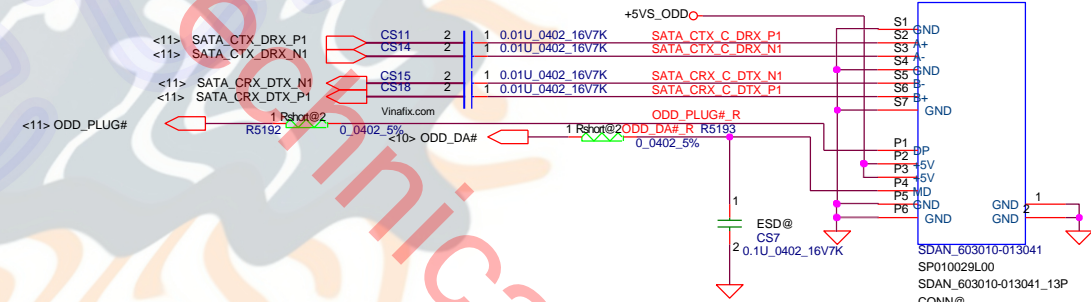
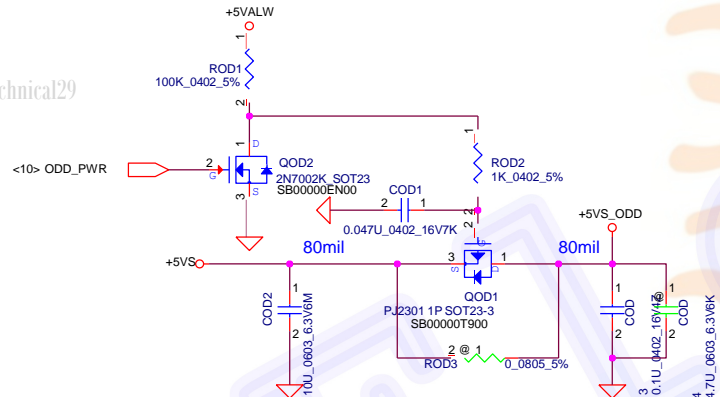
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| | | | | Date | Friday, January 05, 2018 |
| | | | | Sheet | 36 of 36 |

2.5" SATA HDD

<PV> change short pad



SATA ODD

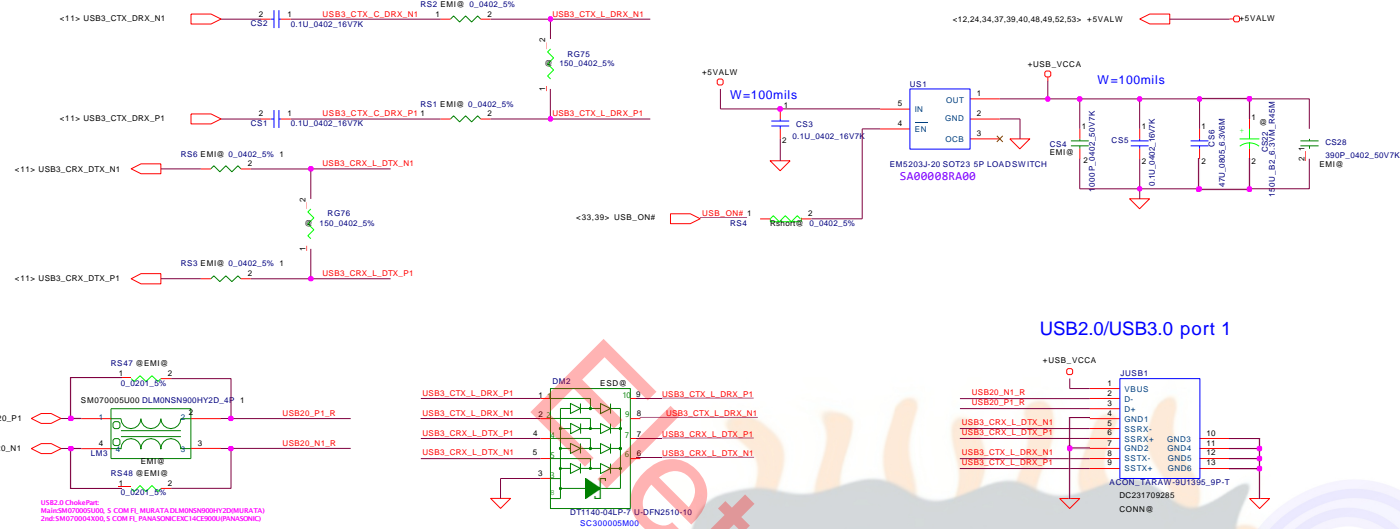


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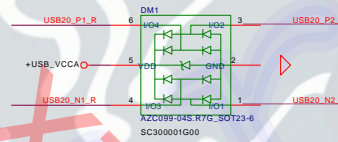
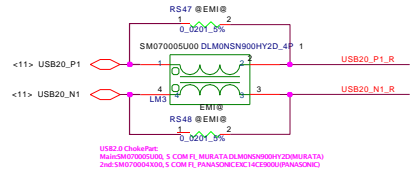
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| | | | | Date | Friday, January 05, 2018 |
| | | | | Sheet | 37 of 39 |

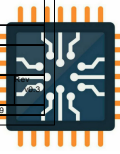
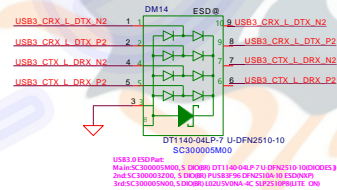
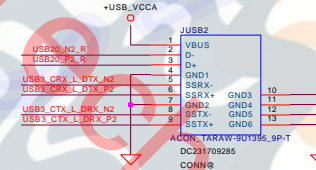
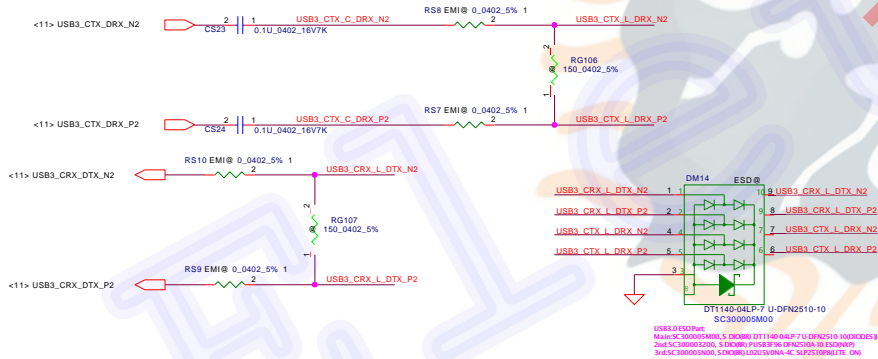


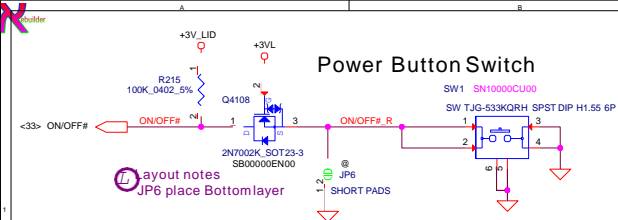


USB2.0/USB3.0 port 1

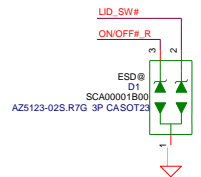


USB2.0/USB3.0 port 2

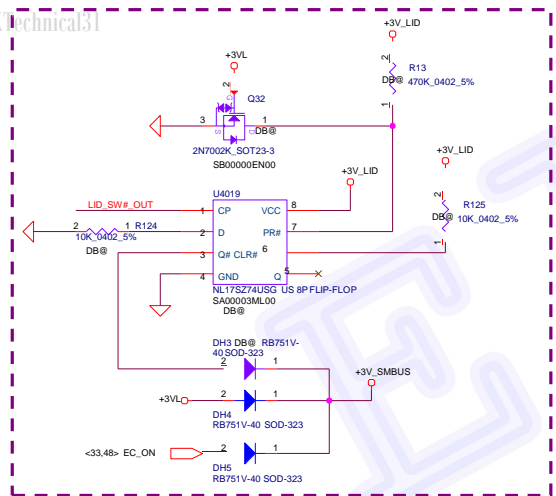
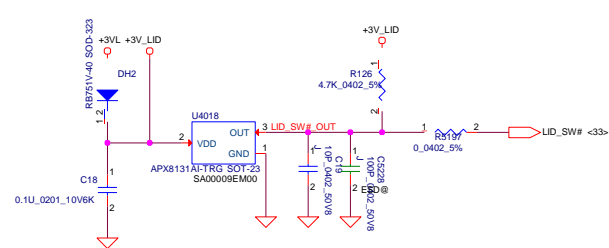




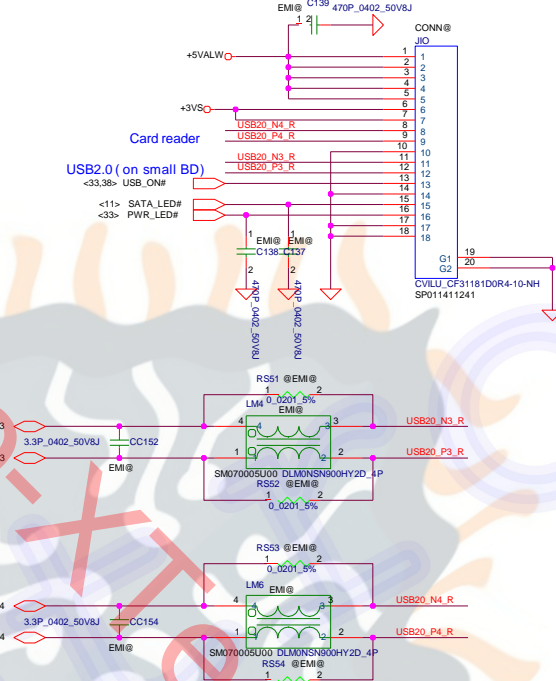
ESD Diode



Lid Switch (Hall Effect Sensor)



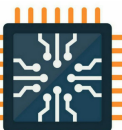
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

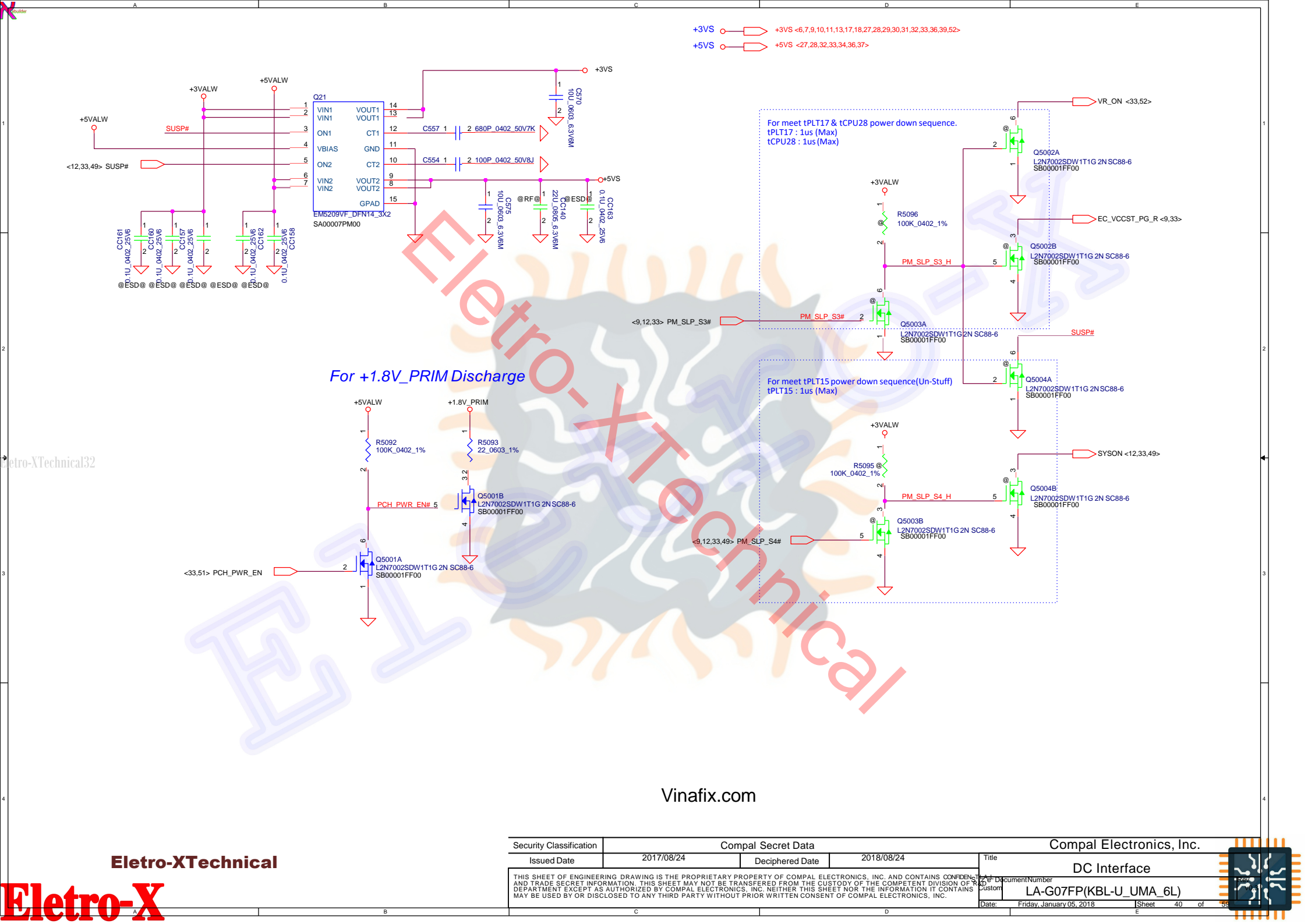


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| LA-G07FP(KBL-U_UMA_6L) | | | | Sheet 39 of 59 |





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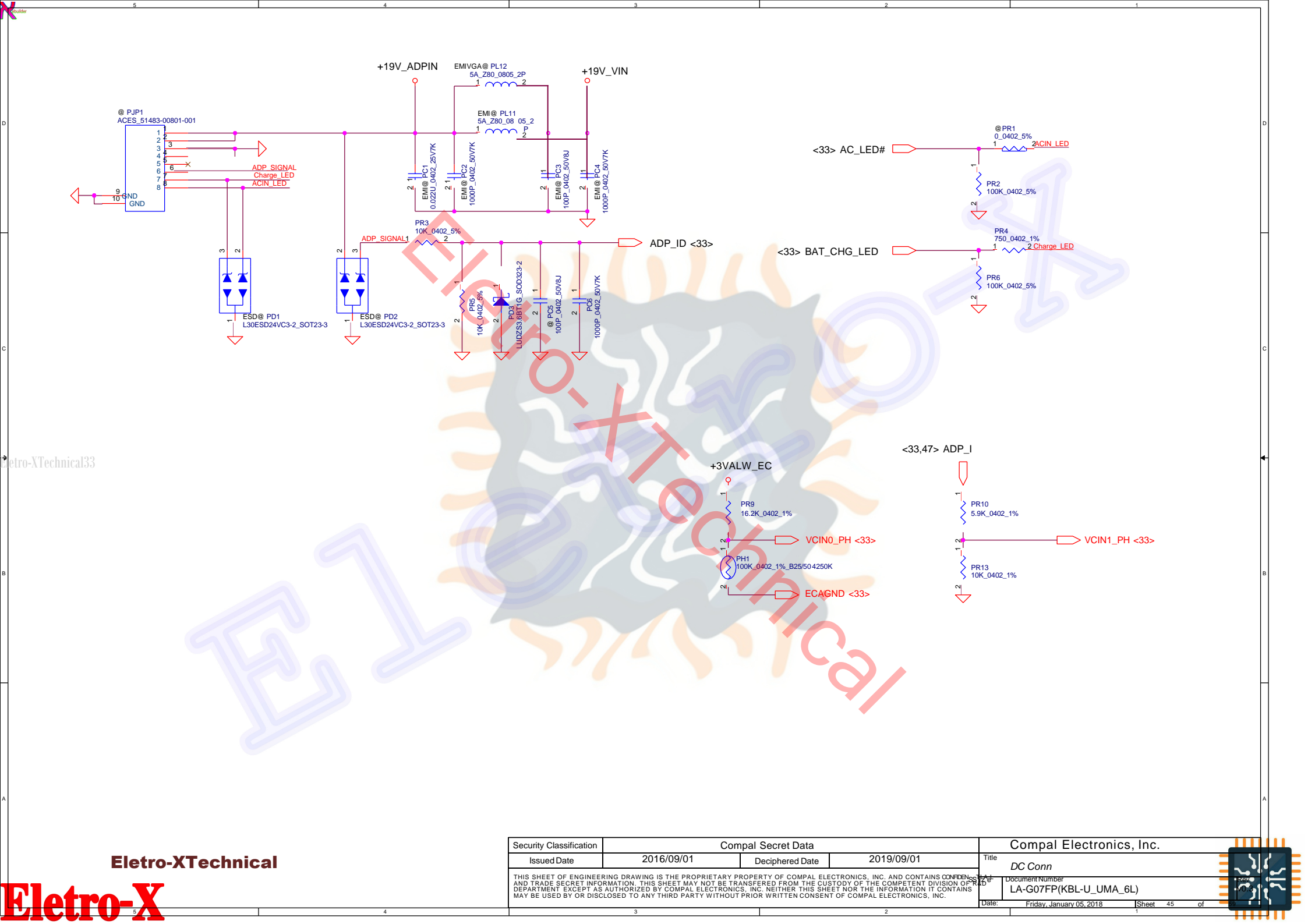
Vinafix.com

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Eleetro-X

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| | | | | Customer | LA-G07FP(KBL-U_UMA_6L) |
| | | | | Date | Friday, January 05, 2018 |
| | | | | Sheet | 40 of 40 |



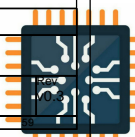


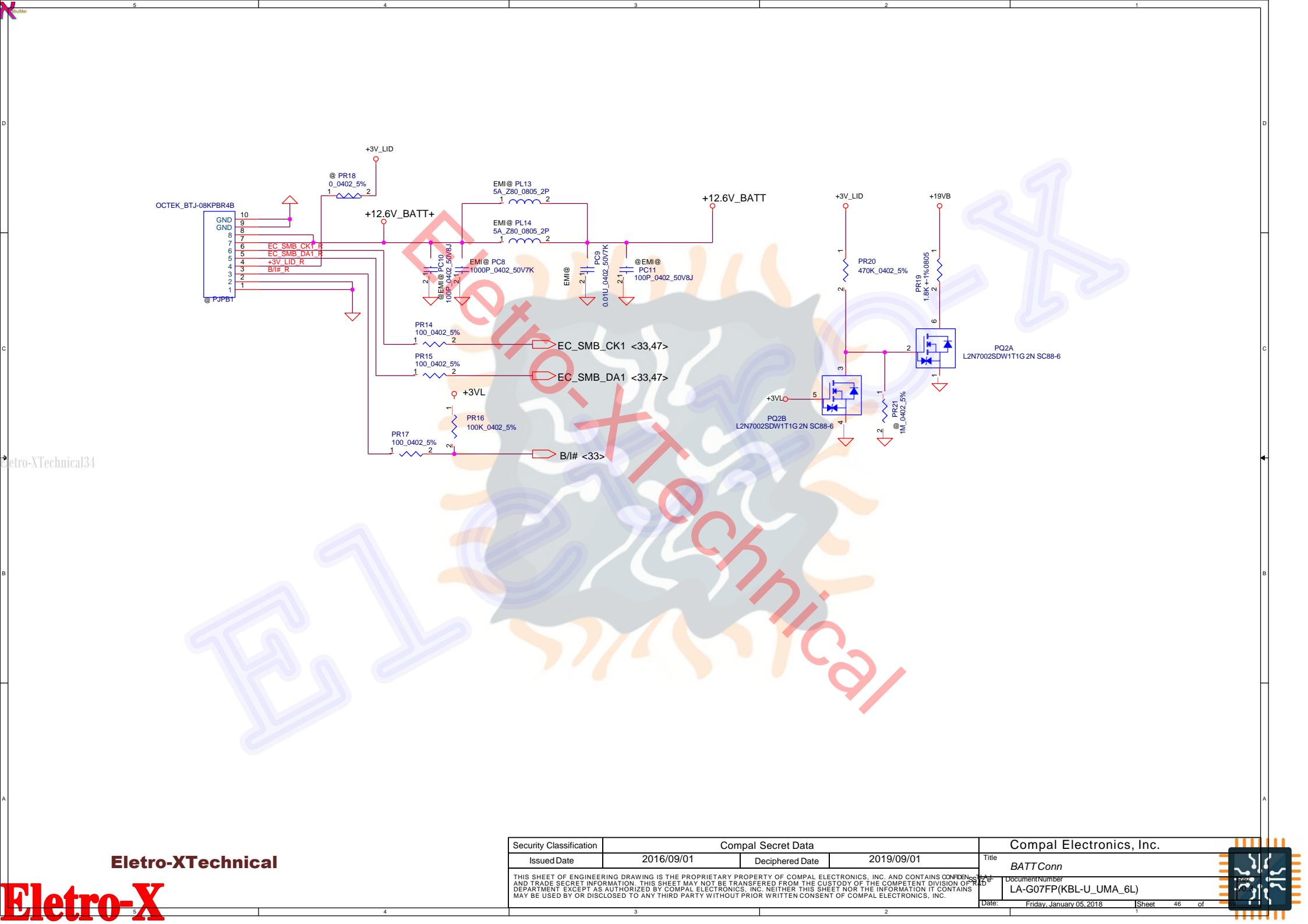
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| Title | DC Conn |
| Document Number | LA-G07FP(KBL-U_UMA_6L) |
| Date: | Friday, January 05, 2018 |
| Sheet | 45 of |



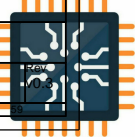


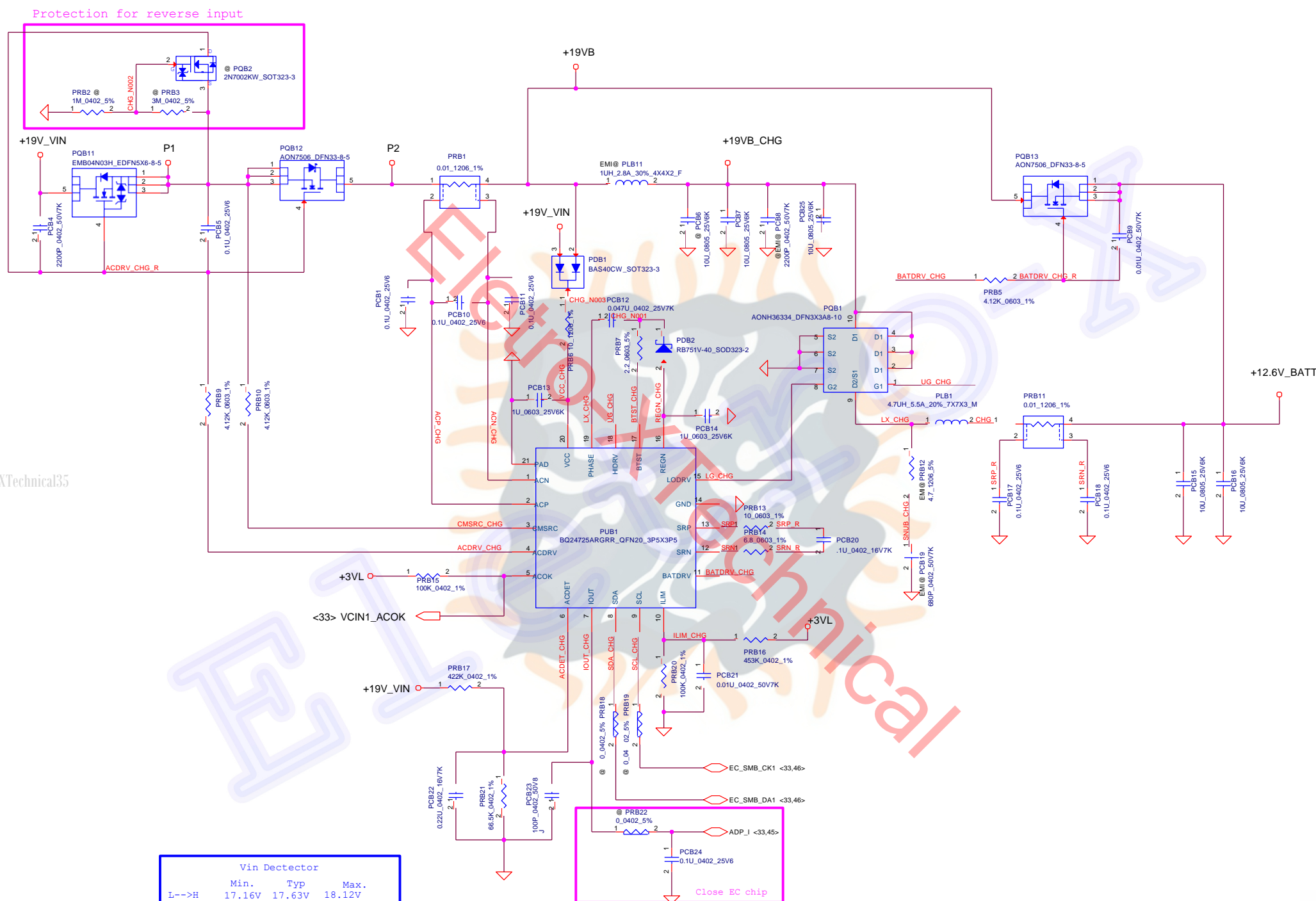
Eletr-X-Technical34

Eletr-X-Technical

Eletr-X

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| | | | | Date: | Friday, January 05, 2018 |
| | | | | Sheet | 46 of |






| | Vin Dectector | | |
|-------|---------------|--------|--------|
| | Min. | Typ | Max. |
| L-->H | 17.16V | 17.63V | 18.12V |
| H-->L | 16.76V | 17.22V | 17.70V |

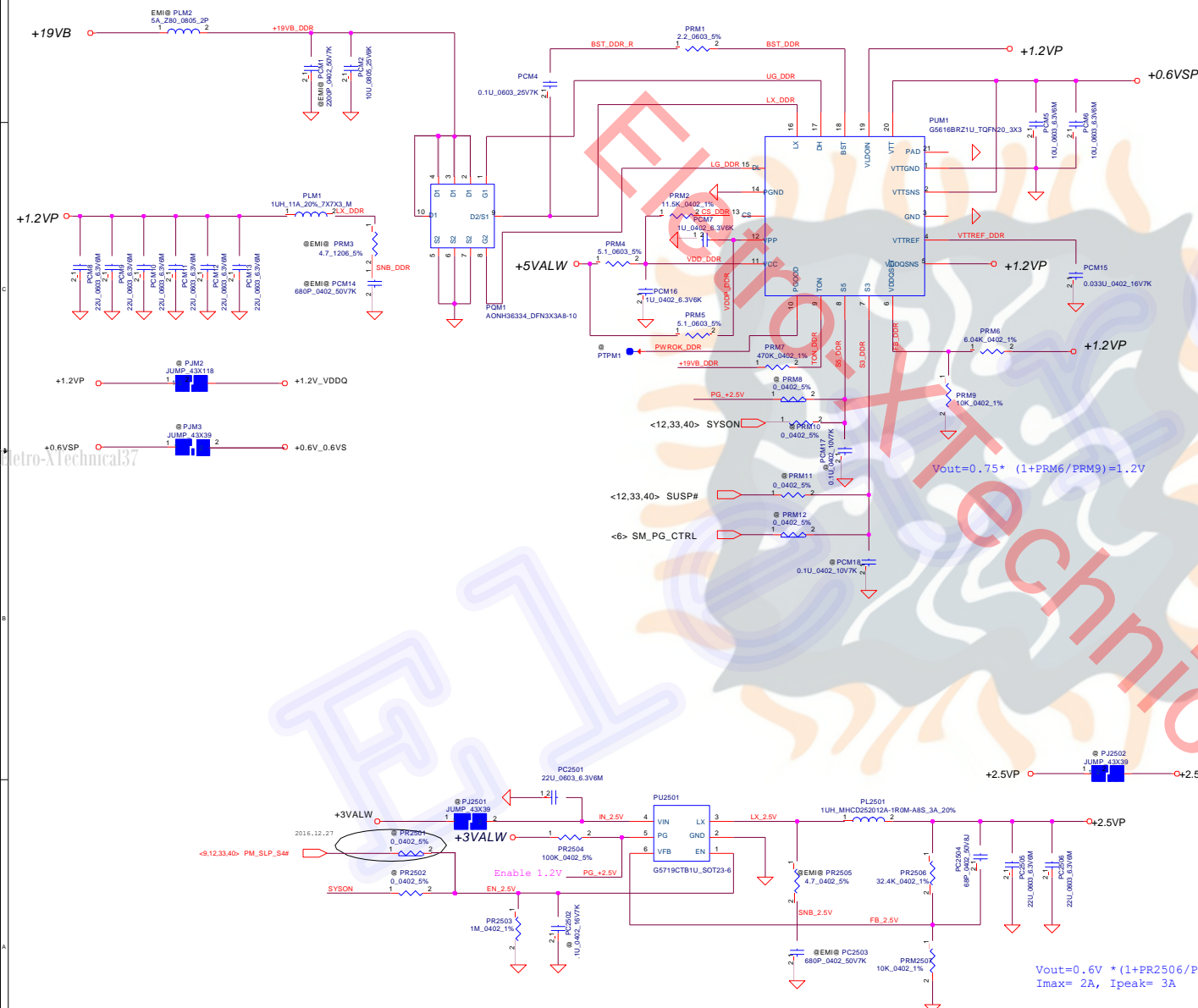
Technical

VILIM = 20*ILIM*Rsr
 ILIM = $3.3 \times 100 / (100 + 620) / 20 / 0.02$
 = 2.291 A

Eleto-XTechnical

Eleto-X

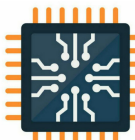
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| | | | | Date: | Friday, January 05, 2018 |

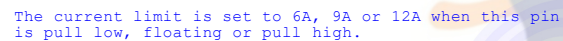


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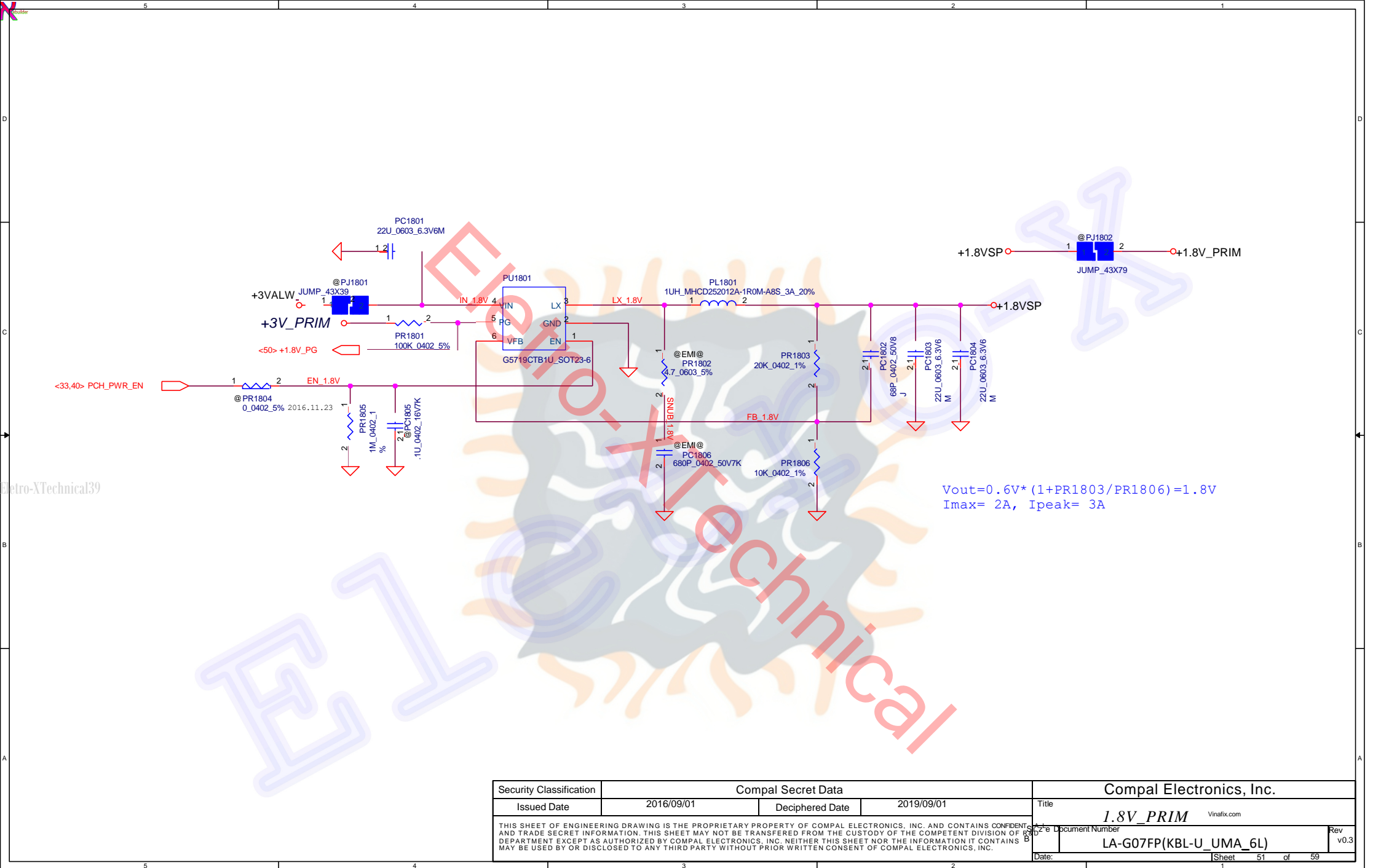
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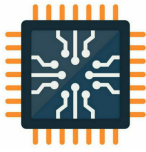


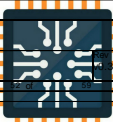
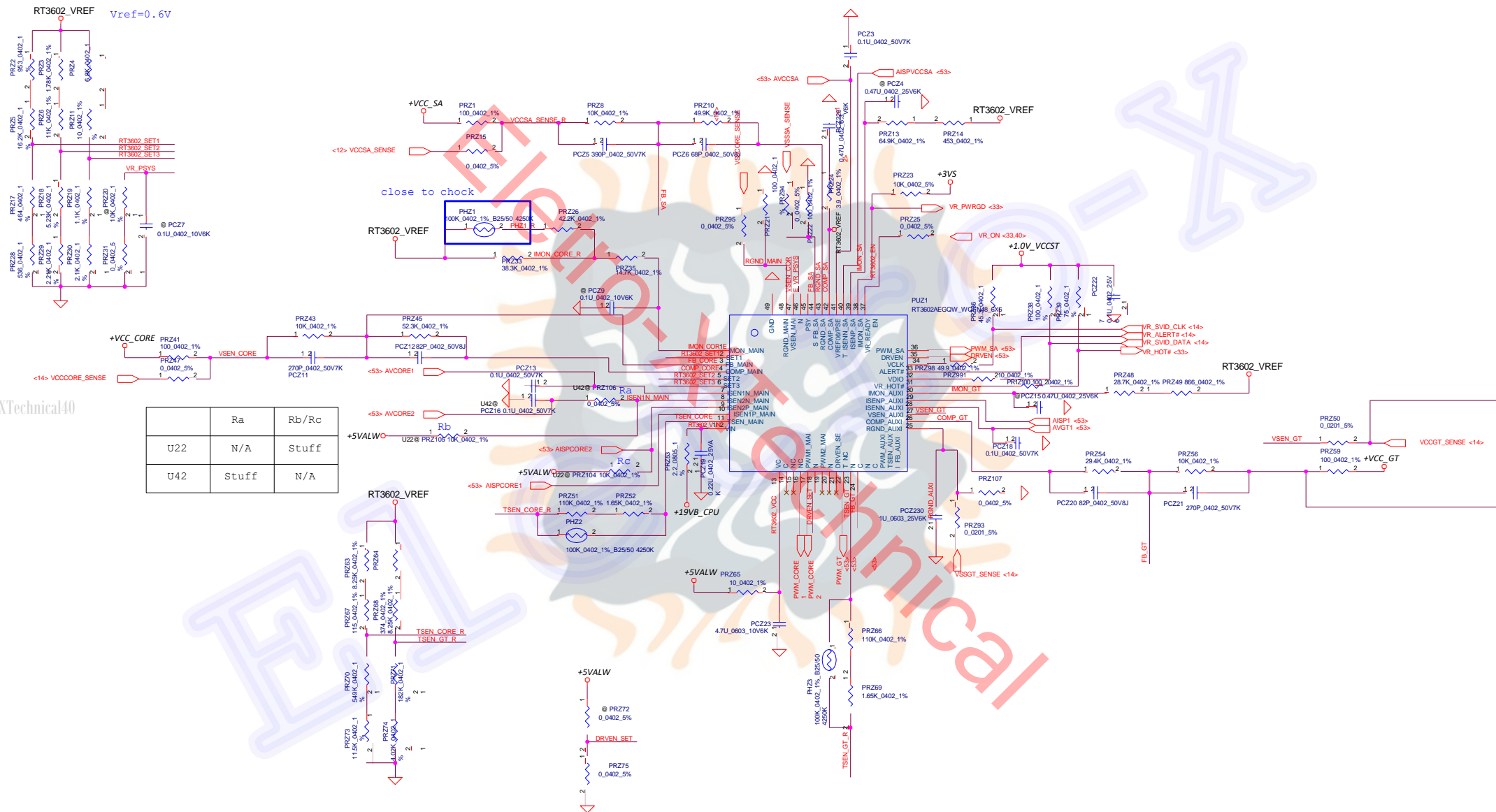


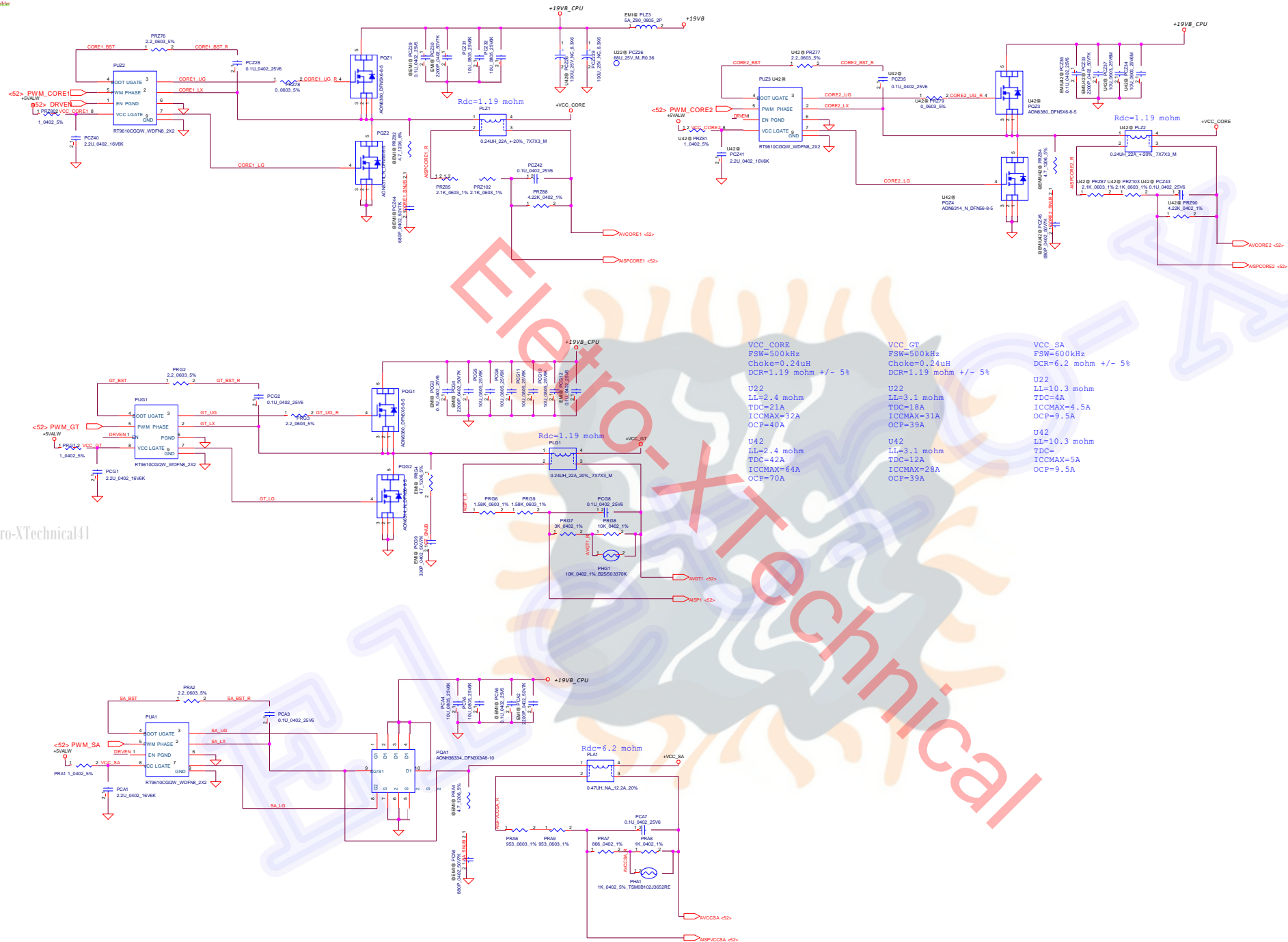
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